New Prospects for Electrostatic Data Storage Systems

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1 Introduction

Magnetic data storage is a unique technology which has maintained an impressive bit density growth during the past few decades. It seems, however, that this growth will saturate somewhere near 100 Gbits/in^2, due to several fundamental factors – see, e.g., Ref. [2]. Recognition of this situation has triggered a wave of research in search of alternative technologies which would enable the current data storage scaling trend to continue after the magnetic systems run out of steam.

The natural candidate for an alternative technology is electrostatic data storage, where a digital bit is retained in the form of a minute (few-electron) charge of a small metallic grain or a group of grains. However, earlier attempts to implement such storage systems ran into several problems, including:

- the lack of sensitive and fast solid state electrometers for reading heads, and
- low speed of write/erase process.

During the past decade, the situation with the first problem has been radically improved due to the invention [3], demonstration [4], and gradual improvement (see, e.g., review [5]) of single-electron transistors (SET). These devices may serve as very good electrometers, with experimentally demonstrated charge sensitivity (at low temperatures) better than 10^{-5} $e/\sqrt{\text{Hz}}$ [6]. Recently, the first operational room-temperature SET was demonstrated [7]. Though the charge sensitivity of room-temperature SETs has not yet been measured, theory [8] predicts that beyond the $1/f$ noise range it may be of the order of 10^{-7} $e/\sqrt{\text{Hz}}$. This would be sufficient for readout of a few-electron signal at a very high (GHz-scale) speed.

Therefore the write/erase speed seems to have become the key problem for the practical introduction of electrostatic storage systems. We have carried out a theoretical analysis of various possible solutions to this problem, and run into what we believe is a very promising opportunity. Its brief description is the objective of this report.

2. Crested Tunnel Barriers

The most evident candidate for the write/erase process is Fowler-Nordheim tunneling, similar to that used in floating-gate memories [9]. The tunnel barrier should have negligible tunneling (corresponding to a charge retention time of a few years) for relatively low voltage V applied to the barrier by the stored charge. On the other hand, in the write mode the applied voltage should suppress the barrier to such an extent that tunneling current recharges the charge storing grains quickly. Simultaneously, this voltage should be small enough to avoid tunnel barrier degradation.
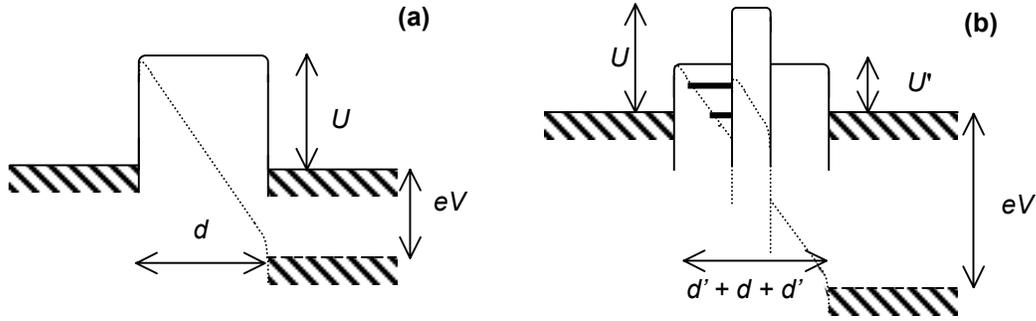
Figure 1. Conduction band edge diagrams of (a) - typical uniform barrier; and (b) - crested layered barrier. Dashed lines show the barrier tilting caused by applied voltage V. Thick horizontal lines in (b) show (schematically) the position of resonant electron subbands enabling resonant tunneling

The usual uniform tunnel barriers (Fig. 1a), made typically of silicon dioxide, cannot satisfy these two conditions simultaneously. Thin curves in Fig. 2 show the current density j and the grain recharging time scale $\tau(V) \equiv C_0V/j(V)$ as functions of voltage V for two typical values of SiO_2 barrier thickness. (The current has been calculated using the standard quasiclassical approximation, in the assumption of the isotropic and parabolic dispersion law for electrons both in the source conduction band and under the barrier. C_0 is the capacitance per unit area of the tunnel barrier.)
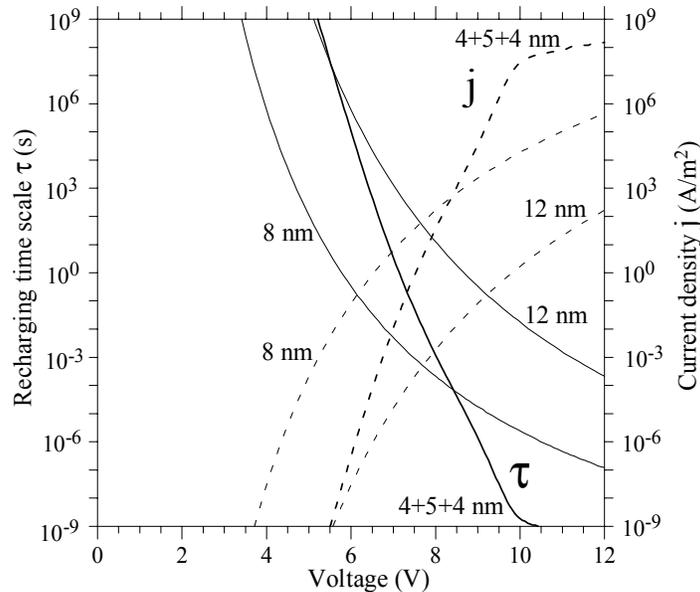

Figure 2. Tunneling current density j (in A/m^2, dashed lines) and the floating gate recharging time scale τ (in seconds, solid lines) for the barriers shown in Figs. 1a and 1b, as functions of applied voltage V, calculated using the quasiclassical theory. Thin lines: uniform barriers with parameters corresponding to $n^+Si/SiO_2/n^+Si$ ($U = 3.2$ eV, $m = 0.3$ m_0, $d = 8$ nm and 12 nm). Thick lines: trilayer crested barrier with parameters corresponding to $n^+Si/Si_3N_4/AlN/Si_3N_4/ n^+Si$ ($U' = 2.0$ eV, $m'= 0.2$ m_0, $\varepsilon' = 7.5$, $d' = 4$ nm;

U = 3.6 eV, m = 0.48 m_0, ε = 8.5, d = 5 nm). It is quite possible that crested barriers using other combinations of materials may have even better performance.

The results show that, for example, a 8-nm-thick barrier may provide a 10-year retention time (~3×10⁸ s) for voltages below ~ 3.5 V, but the write time at the largest acceptable electric field E_{max} ~ 10 MV/cm [10] is above 1 μs. A change in the barrier thickness d to either side does not help (see, e.g., the results for d = 12 nm in Fig. 2), neither does a change in the barrier height. This relatively weak dependence of the barrier transparency on the electric field is due to the fact that the highest part of the barrier, closest to the electron source, is only weakly affected by the applied voltage: U_{max} (V) $\approx$ U_{max} (0) - see the dashed line in Fig. 1a.

Now consider a "*crested*" layered barrier (Fig. 1b) [11, 12]. Solid curves in Fig. 2 show that the current through this barrier changes much faster, so that a sufficiently long retention time at low voltages may be combined with 1-ns-scale write/erase at moderate electric fields (about 7 MV/cm). The physical reason for this dramatic improvement is that in the crested barrier the highest part (in the middle) is pulled down by the electric field very quickly: U_{max} (V) $\approx$ U_{max} (0) - $eV/2$ – see dashed curves in Fig. 1b. As a result, the barriers may enable 1-ns-scale write/erase in electric fields as low as 7 MV/cm. In these low fields the barriers should have extremely high endurance, allowing a virtually unlimited number of write/read cycles.

3. ESTOR

Figure 3 shows the possible electrostatic data storage system (ESTOR) which combines the unique charge sensitivity of single-electron transistors and speed of recharging through crested barriers [11, 17]. The system includes a read/write head with an SET preamplifier loaded on a FET amplifier at a distance of a few microns. The data bits are stored as few-electron charges ($Q/e = n$ ~ 30) trapped in nanoscale conducting grains deposited on the top of a crested tunnel barrier. Since the charge is relatively large, and is stored in a few (~ 30) grains, their exact shape and location are not important, so the storage medium does not require nanofabrication: the grains of random size may be deposited, e.g., by metal evaporation.

Bit writing is achieved by the application of high voltage V_W in the moment when the head is passing over the specified location (at writing, V_R = 0, so that the SET is deactivated and works just as a single conductor delivering voltage V_W to the tip). The voltage suppresses the tunnel barrier, and inserts the charge into the group of grains. Nondestructive readout is achieved by the SET activation (V_W = 0, $V_R \neq$ 0), turning the device into a sensitive electrometer [19].

Estimates show that with a 15-nm tip-to-substrate distance (typical for the advanced magnetic storage systems), the ESTOR system is capable of a density above 1 Tbit/in², i.e. at least one order of magnitude higher that the apparent upper density limit for magnetic systems [1]. The use of crested barriers may provide a very broad bandwidth of write/erase, up to 1 Gigabit per second per channel. The maximum reading speed, limited by the internal noise of the SET (with a signal-to-noise ratio of, say, 100), is even higher.
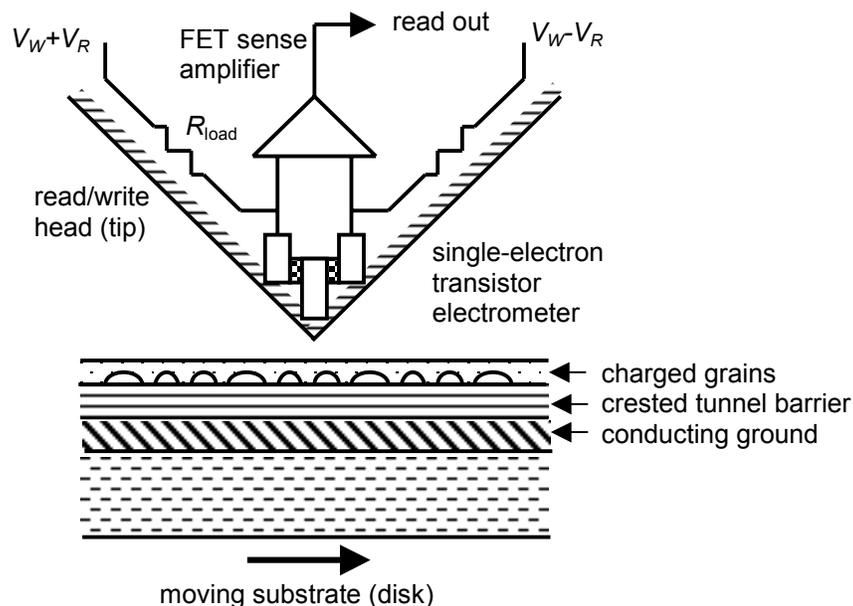
Figure 3. A possible ultradense electrostatic recording system ("ESTOR")

The recent experiments at Lucent Technologies [20] may be considered as the first step toward the implementation of the ESTOR. In these experiments a SET electrometer fabricated on a scanning probe was used for the detection of single-electron charges on Si and GaAs substrates. In these preliminary experiments, there was no FET amplifier close to the SET output, so that the available measurement bandwidth was very low. However, recently several groups have demonstrated the possibility of broadband SET/FET integration (so far, at low temperatures). It seems that the unification of these achievements with the progress in fabrication of room-temperature SET [7] and the standard mechanics developed for magnetic hard drives opens a straightforward way toward the implementation of practical ultradense electrostatic data storage systems.

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[9] *Nonvolatile Semiconductor Memory Technology*, ed. by W.D. Brown and J.E. Brewer (New York: IEEE Press, 1998).

[10] In stronger fields, the hopping ("Frenkel - Poole") conductance via deep localized states becomes essential, and eventually leads to the barrier degradation, sharply limiting the barrier endurance, i.e. the maximum number of write/erase cycles [9].

[11] K.K. Likharev. *Appl. Phys. Lett.* **73** (1998) 2137-2139. In that work, the effect of resonant tunneling via electron subbands (which are naturally formed in layered barriers in high electric fields – see Fig. 1b) has been ignored. More adequate calculations [13] have, however, confirmed the basic conclusions of Ref. 16; the resonant tunneling effect may be compensated by an increase of the side layer thickness.

[12] A positive effect of "graded" or "stepped" tunnel barriers on the speed of electron emission was noticed [14-16], and its use in floating gate memories has been suggested [14, 16], long ago. However, the authors of those works considered asymmetric triangular barriers. Though the injection characteristics of such barriers may be even better than those of symmetric crested barriers [11], this is only true for one current direction (say, "write"). The speed of the reciprocal process ("erase") is low, thus excluding the possibility of data storage applications.

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[18] This proximity is necessary to reduce the interconnect capacitance which should be recharged through the high output impedance of the single electron transistor and hence to ensure high readout bandwidth.

[19] For this application, the randomness of the background charge, which is the largest obstacle on the way toward other digital applications of single-electron devices [3], is not important, since it may always be compensated by an additional gate voltage tuned to bias the SET into a point with maximum sensitivity.

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