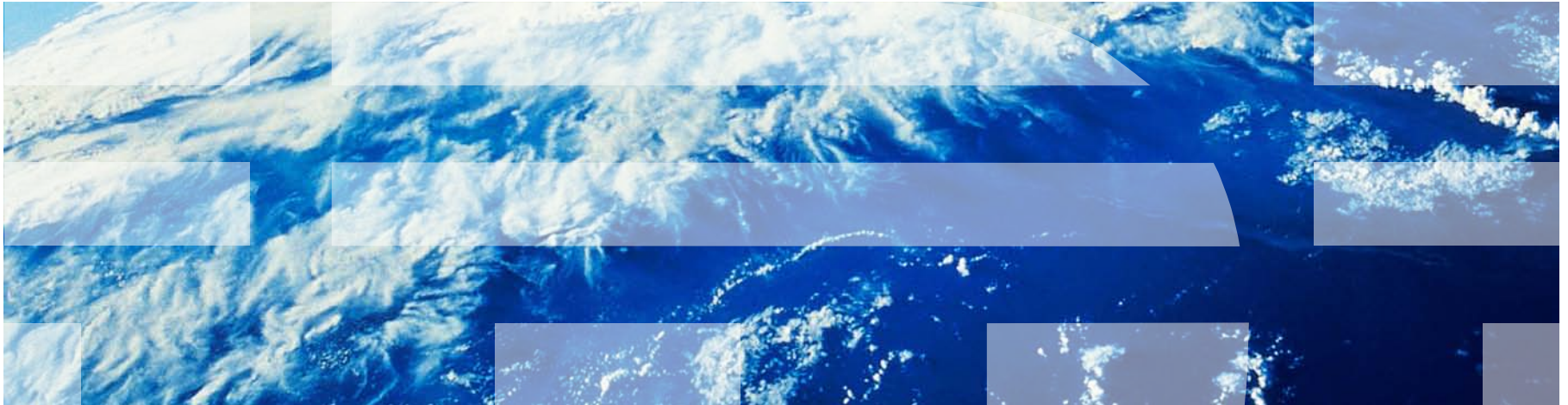


Technology Roadmap Comparisons for TAPE, HDD, and NAND Flash: Implications for Data Storage Applications



Outline

- **Business as Usual Areal Density Increase → 40% per Year**
- **Premise: The annual rate of areal density increases for TAPE will likely exceed the annual rate of areal density increases for NAND and HDD**
 - TAPE bit cell is large and paths for scaling to higher bit densities exist
 - NAND bit cells and HDD Patterned Media bit cells are approaching nanoscale issues in minimum feature lithography requirements
 - NAND bit endurance or bit retention and HDD bit stability are approaching kT fluctuation issues driven by the small volume of the bit cells at high areal densities (< 1900 nm² bit cell area)
- **Comment: TAPE, NAND, and HDD will continue to offer complementary storage solutions**
- **Implications for TAPE: TAPE volumetric density will increase, allowing for new tape opportunities in a more cost sensitive storage environment**
- **A Possible Annual Areal Density Growth Scenarios**
 - 20% for HDD
 - 20% to 30% for NAND Flash
 - 40% to 80% for TAPE

Storage Component Landscape

▪ Three Components

- HDD ~ 500 GB capacity 630 million units/yr (large commodity base)
- NAND Chip ~ 4 GB capacity 4 billion units/yr (large commodity base)
- LTO Tape Cartridge ~ 800 TB capacity 24 million units/yr (**no commodity base**)

▪ The Industries

	2010	2011
HDD Revenue	\$33.5 B	\$33.5 B
HDD PB Shipped	330000 PB	330000 PB
HDD \$/GB Shipped	\$0.10/GB	\$0.10/GB
NAND Revenue	\$18.5 B	\$21.5 B
NAND PB Shipped	10,400 PB	18,600 PB
NAND \$/GB	\$1.77/GB	\$1.16/GB
TAPE LTO Cartridge Revenue	\$0.7 B	\$0.7B
TAPE LTO Cartridge PB Shipped	15,300 PB	17,800 PB
TAPE LTO Cartridge \$/GB	\$0.046/GB	\$0.038/GB



***Thailand Floods
Industry Consolidation***



***Transition from 30 nm
to 20 nm Lithography***



***Introduction of LTO5
Tape Generation***

Areal Density Overview (a moving target -- concentrate on YE 2011 values)

▪ HDD (20% - 30%) / Year

- YE 2009 530 Gbit/in²
- YE 2010 635 Gbit/in²
- Mid 2011 750 Gbit/in²



▪ HDD (3.5" Platter)

- 750 GB → 1.0 TB

▪ TAPE (40% / Year)

- Mid 2008 1.0 Gbit/in²
- Mid 2010 1.2 Gbit/in²
- Mid 2011 3.2 Gbit/in²



▪ TAPE (LTO like Cartridge)

- 1.5 TB → 4.0 TB

▪ NAND (40% / Year)

- Mid 2008 200 Gbit/in²
- Mid 2010 330 Gbit/in²
- Mid 2011 550 Gbit/in²



▪ NAND (Chip)

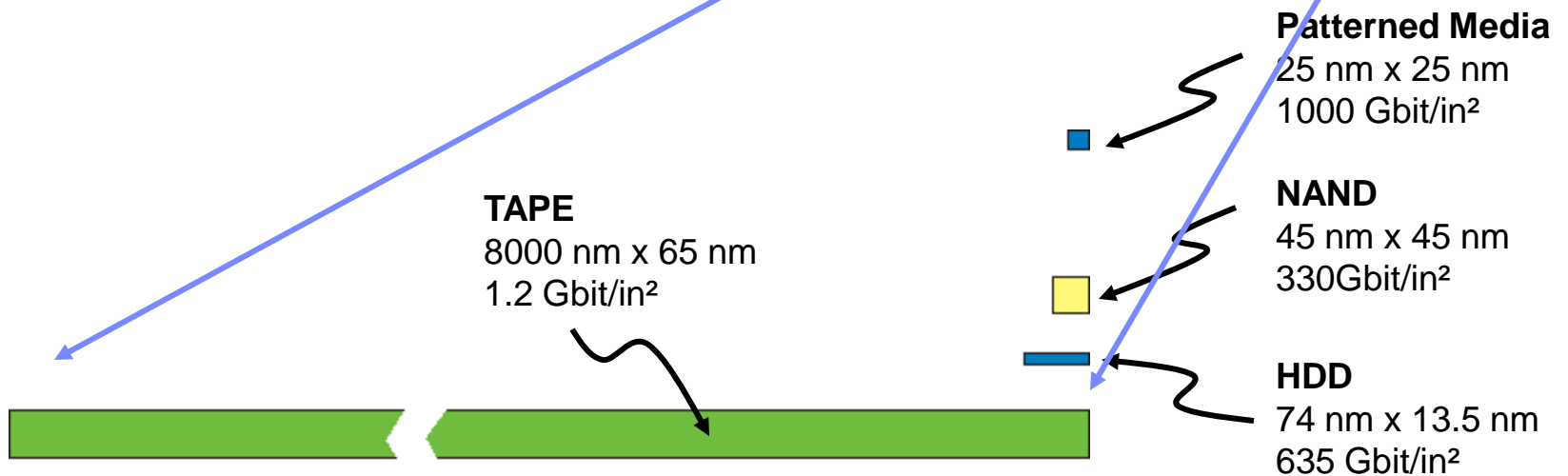
- 8 GB → 8 GB with 40% less area)

Storage Bit Cells and Extendability

- **Scaled Bit Cells**



- **Magnified View of Scaled Bit Cells**

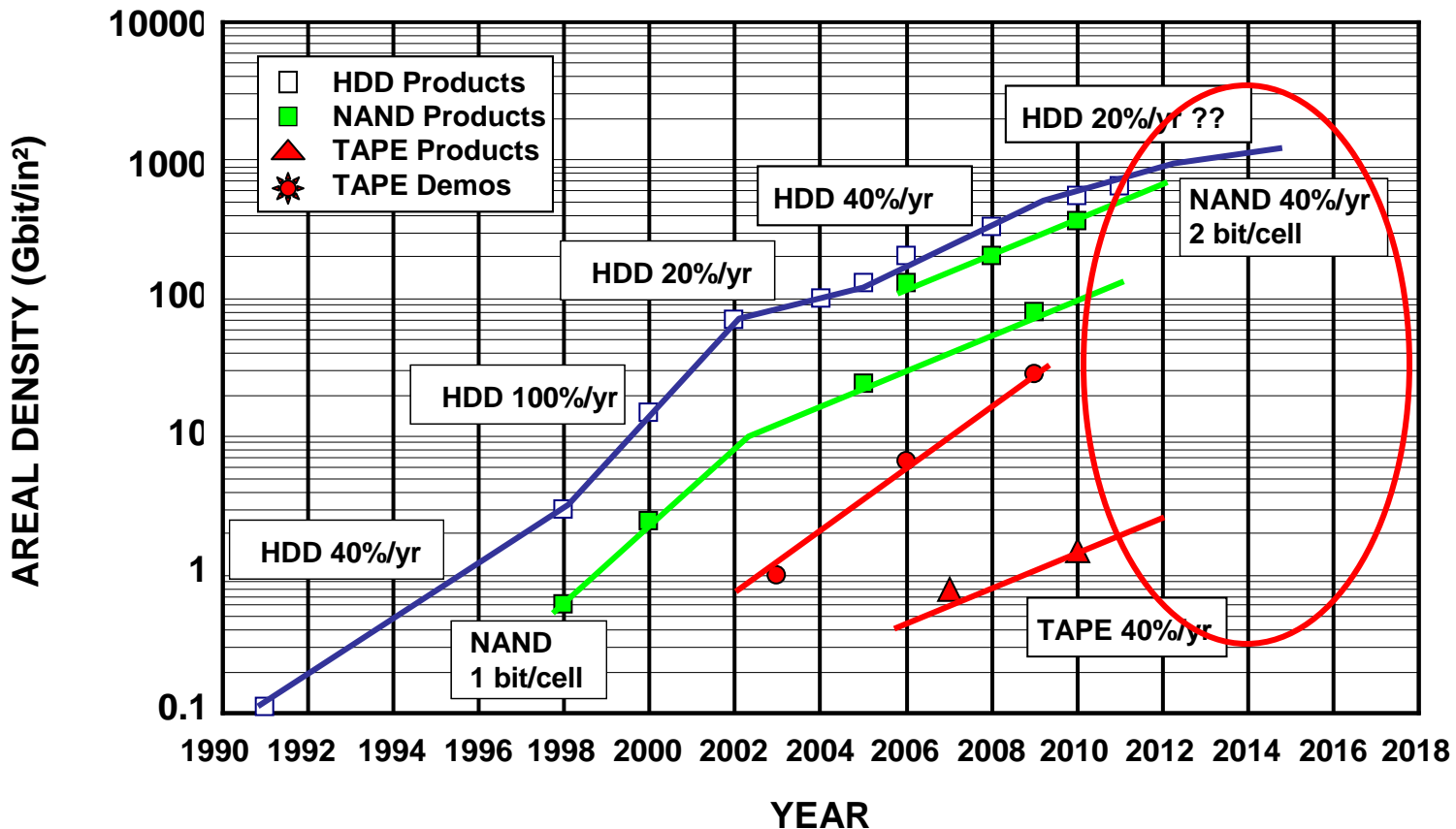


Outline

- **Areal density landscape for TAPE, HDD, NAND**
- **Implications of continued 40% annual areal density increases**
- **Bit cell landscape and lithography roadmaps**
- **Volumetric density examples**
- **TAPE , NAND, HDD landscapes**
- **Areal density increase scenarios for the next 4 year period**
- **Conclusions**

Storage Device Density Landscape – A History

- **HDD**
 - 1998 – 2002 density increases at 100% per year (GMR)
- **TAPE**
 - Sustained 40% density increases with demos showing potential for greater increases
- **NAND**
 - 2005 -- transition to 2 bit/cell technology (endurance sacrifice)



Bit Cell Implications for 40% Annual Areal Density Increases

TECHNOLOGY METRIC	2010	2014 (40% / Yr)
<u>TAPE</u>		
-- Areal Density	1.2 Gbit / in ²	4.8 Gbit / in ²
-- Bit Length	8000 nm	2000 nm
-- Bit Width	65 nm	65 nm
-- Minimum Feature	4000 nm	1000 nm
<u>HDD</u>		
-- Areal Density	635 Gbit / in ²	2500 Gbit / in ²
-- Bit Length	74 nm	19 nm
-- Bit Width	13.5 nm	13.5 nm
-- Minimum Feature	37 nm	10 nm
<u>NAND Flash</u>		
-- Areal Density	330 Gbit / in ²	1300 Gbit / in ²
-- Bit Length	45 nm	20 nm
-- Bit Width	45 nm	20 nm
-- Minimum Feature	25 nm	12 nm

Nano Patterning Landscape

- International Technology Roadmap for Semiconductors (ITRS) Update on Minimum Feature Processing – July 14, 2010

	2010	2011	2013	2016
NAND	32 nm¹	28 nm	23 nm	16 nm
DRAM	45 nm	40 nm	32 nm	23 nm
MPU/ASIC	45 nm	38 nm	27 nm	19 nm

1. Intel/Micron reports 25 nm 2Q 2010

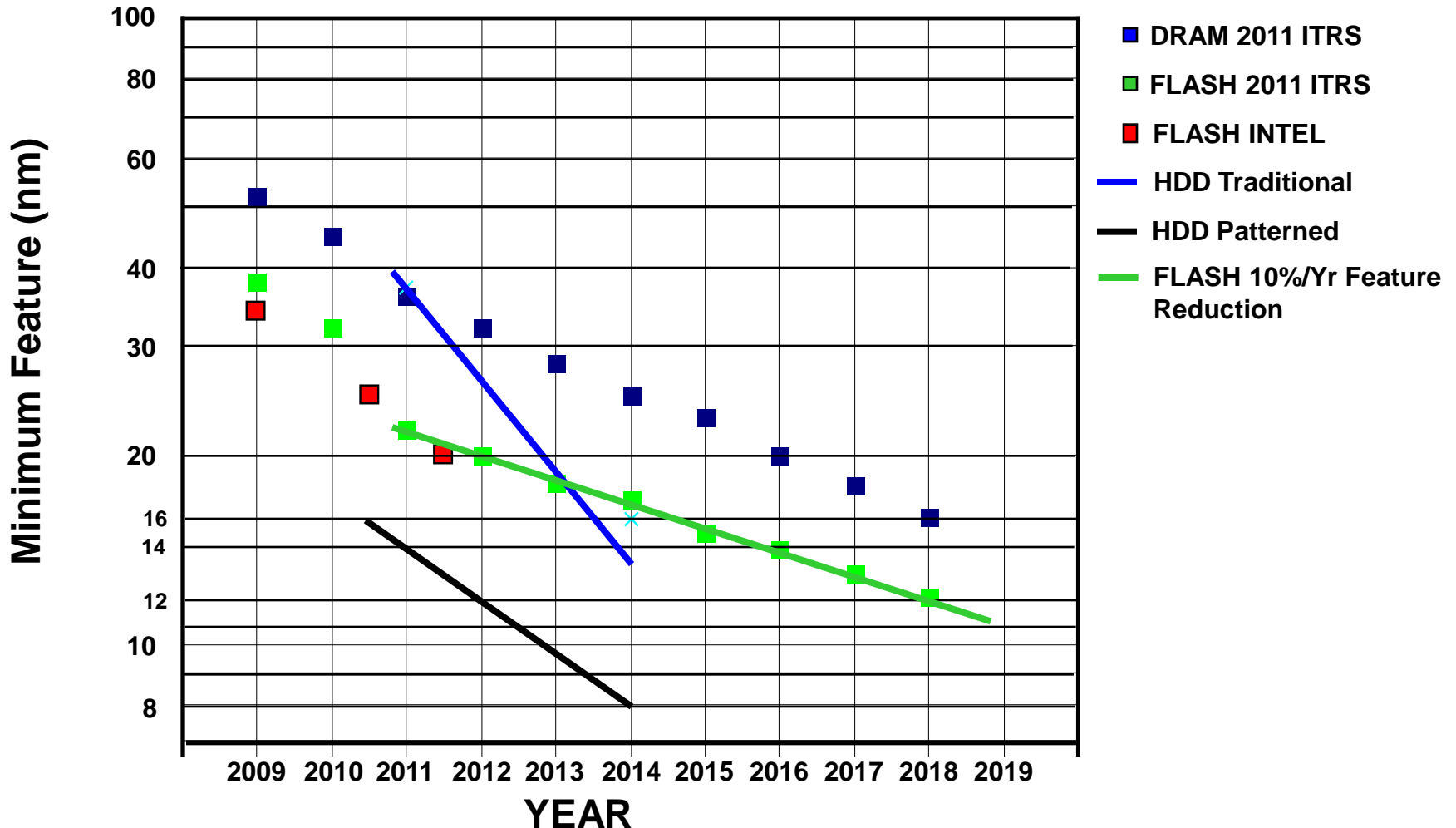
- International Technology Roadmap for Semiconductors (ITRS) Update on Minimum Feature Processing – July 13, 2011

		2011	2013	2016
NAND		22 nm²	18 nm	15 nm
DRAM		36 nm	28 nm	20 nm
MPU/ASIC		38 nm	27 nm	19 nm

2. Intel/Micron reports 20 nm 2Q 2011

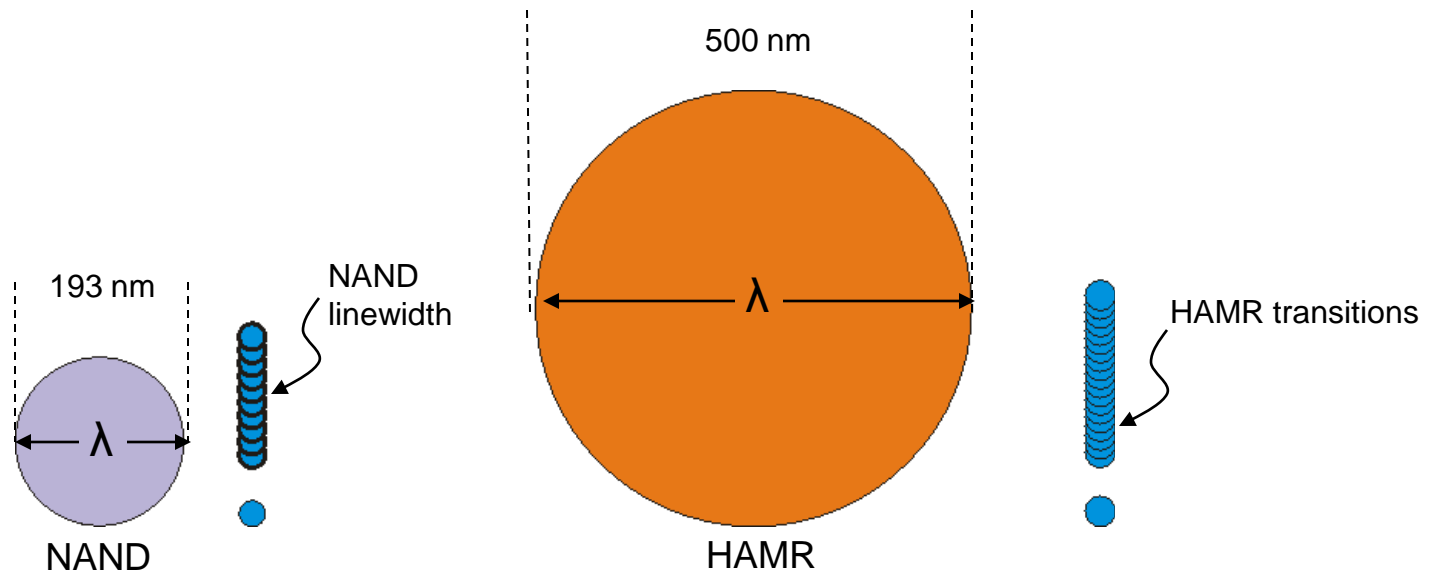
Lithography Roadmaps

- Minimum feature typically reduced by 12% per year
- Intel/Micron has consistently exceeded ITRS goals



NAND and HAMR Optics -- Today

- **NAND uses 193 nm wavelength light to resolve 20 nm features**
 - Phase shift masking
 - Immersion lithography
 - Double exposure at 2X line pitch
 - Chemically amplified resists
- **HAMR uses ~ 500 nm wavelength light to resolve 100 nm features today and 35 nm features for 2 Tbit/in² in the 2014 time frame**
 - Waveguide propagation
 - Waveguide termination with aperture feature (minimum feature)
 - Near field thermal effects
 - Media layer heat sinking

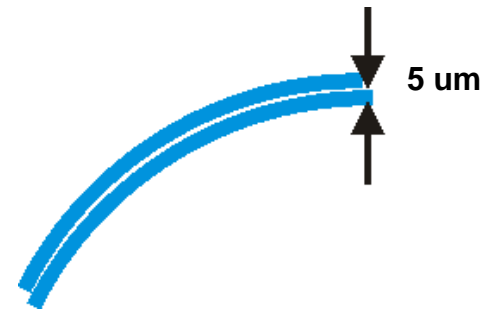


Local Volumetric Density Comparisons for 2010

▪ Packaging and Media Thickness and Substrate Thickness

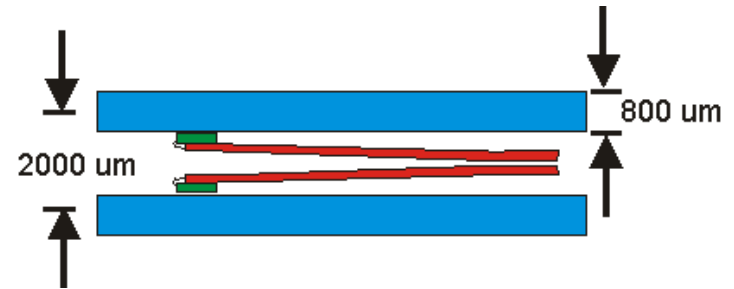
▪ Tape

- **1.2 Gb/in²**
- 5 μm tape thickness
- Local Volumetric Density = **6.0 Tb/in³**



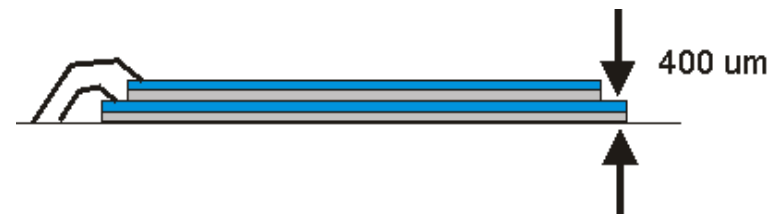
▪ Disk

- **635 Gb/in²**
- ½ disk thickness = 400 μm
- Slider thickness = 250 μm
- Disk to disk separation = 2000 μm
- Local Volumetric Density = **15.8 Tb/in³**



▪ NAND

- **330 Gb/in²**
- Thinned substrate thickness = 200 μm
- Stacking spacing = 200 μm
- Local Volumetric Density = **20.1 Tb/in³**



Volumetrics – True Component Level Comparisons

▪ YE 2010

	SSD (FLASH) Drive	HDD (DISK) Drive	LTO5 (TAPE) Cartridge
Capacity	0.5 TB	3.0 TB	1.5 TB
Price	\$1500	\$200	\$50
\$/GB	\$3.00	\$0.07	\$0.03
Components	128 166 mm ² 4GB chips	4-5 87 mm disk platters	1 tape cartridge (12.5 mm x 820 m)
Device Volume	4.2 in ³	24.2 in ³	14.8 in ³
Storage Density	120 GB/in ³	120 GB/in ³	101 GB/in ³



▪ MY 2011

	SSD (FLASH) Drive	HDD (DISK) Drive	LTO5 (TAPE) Cartridge
Capacity	0.5 TB	3.0 TB	1.5 TB
Price	\$1000	\$150	\$50
\$/GB	\$2.00	\$0.05	\$0.03
Components	64 166 mm ² 8GB chips	3-4 87 mm disk platters	1 tape cartridge (12.5 mm x 820 m)
Device Volume	4.2 in ³	24.2 in ³	14.8 in ³
Storage Density	120 GB/in ³	120 GB/in ³	101 GB/in ³



TAPE Landscape – 1.5 TB LTO-5 Tape Cartridge

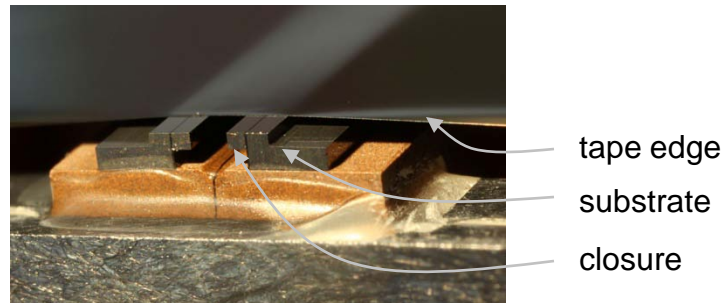
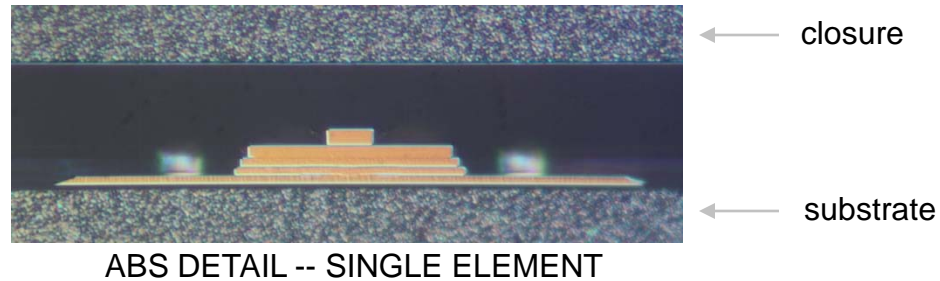
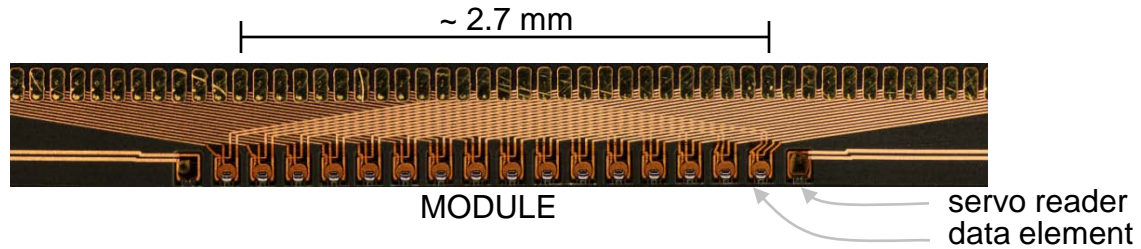
- **Tape data storage capacity achieved using 840 m tape length, 12.8 mm wide, and 6.4 μm thick**
 - Tape surface area in a cartridge ($10.5 \times 10^6 \text{ mm}^2$) is equivalent to 148 12" Si wafers or 1736 3.5" disk surfaces
 - Some surface area utilized for edge guards, servo tracks, leading and trailing tape end lengths leading to surface storage efficiencies of $\sim 65\%$

- **1.5 TB LTO-5 Cartridge Details**
 - Areal Density (Maximum) $\rightarrow 1.2 \text{ Gbit/in}^2$
 - Areal Density (Average) $\rightarrow 0.72 \text{ Gbit/in}^2$
 - Memory Cell Area $\rightarrow 520000 \text{ nm}^2$ or $0.52 \text{ } \mu\text{m}^2$
 - Total Tracks $\rightarrow 1280$
 - Trackwidth $\rightarrow 8100 \text{ nm}$ or $8.1 \text{ } \mu\text{m}$
 - Bit Length $\rightarrow 65 \text{ nm}$
 - Bit Aspect Ratio $\rightarrow \sim 125 \text{ !!!}$
 - TPI, BPI $\rightarrow 3.1 \text{ KTPI}, 385 \text{ KBPI}$
 - Read Width/Minimum Feature $\rightarrow \sim \frac{1}{2} \text{ Trackwidth}, \sim 4.0 \text{ } \mu\text{m}$
 - Memory Cell Area (F^2) $\rightarrow \sim 0.03F^2 \text{ !!!}$

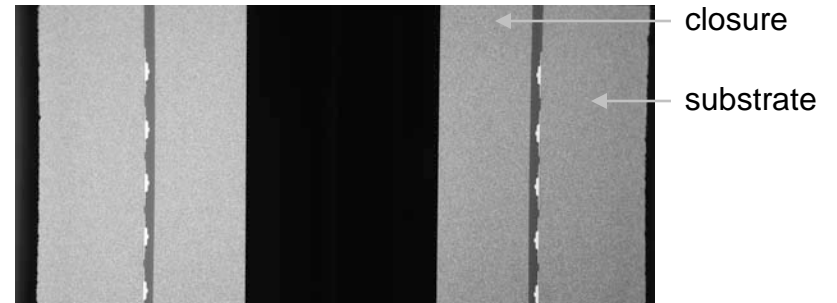
1.5 TB LTO-5 Tape Head

▪ The Head

- 2 16 element read/write modules
- Write on one module, read verify on other module



TWO MODULE HEAD WITH TAPE



ABS DETAIL – TWO MODULE HEAD

Tape Landscape – Anticipated Density Increases

- **Media:**

- Recording demonstrations suggest that tape areal densities in excess of 25 Gb/in² can be supported **(20X)**
- SNR is the issue

- **Head:**

- The recent transition to GMR based sensors provides paths for maintaining amplitude as trackwidth decreases
- Present Trackwidths and MR widths in the 4 um range are **200X** larger than present IC minimum features (20 nm to 25 nm) so lithography limits are non issues

- **Bit Cell:**

- Tape uses HDD BPI values of 5 years ago with HDD TPI values of 12+ years ago so utilizing HDD head expertise will allow for TPI intensive areal density increases
- The volume and the surface area of the bit cell are large so kT fluctuations are minimized

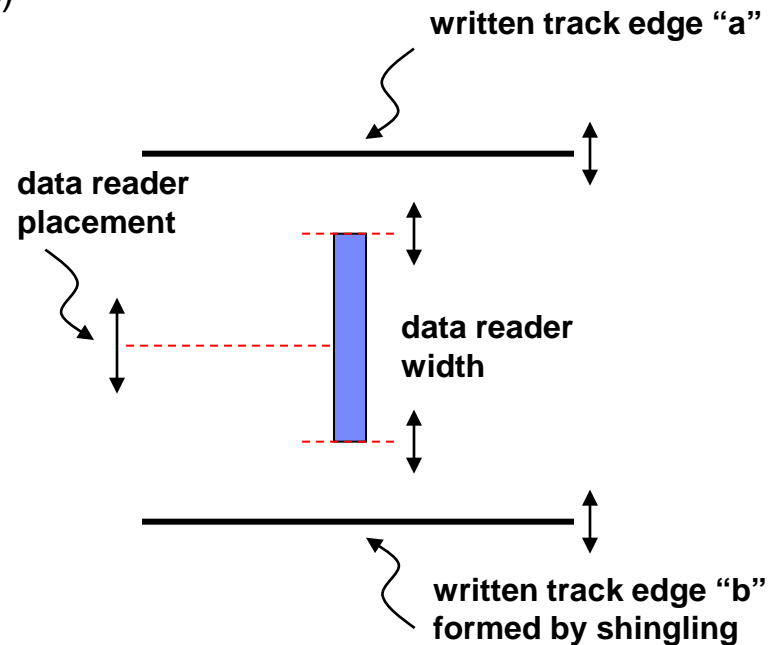
BUT

- **Flexible media and track following**

- **Large “head – tape” spacing (i.e. recession changes during head lifetime)**

Track Following and the MR Width

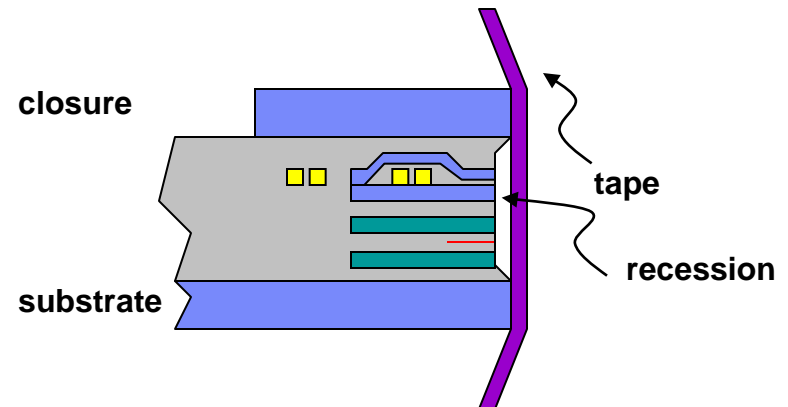
- The read width in a tape head is designed to be smaller ($\sim 4\mu\text{m}$ for an $8\mu\text{m}$ track pitch) than the written track width (write wide – read narrow) in order to accommodate variations in the ability of the sensor to “track” the written track of interest
- Some of these variations do not readily scale with trackwidth!!!
- Tracking Categories
 - Head Positioning (*signal processing opportunities*)
 - Position error signal
 - Write head incursion on adjacent track
 - Tape Dimensional Stability (TDS)
 - Not an issue for HDD ←
 - Environmental (temp and humidity) in ppm
 - Tension
 - If TDS is 500 ppm then tracks on tape written by adjacent elements could move by $0.09\mu\text{m}$ and tape tracks written by element 1 and element 16 could move by $1.35\mu\text{m}$!!
 - Head Wafer Parameters (*good scaling*)
 - Data writer and reader width control
 - Servo reader alignment to data writer and data reader



Head Recession Issues

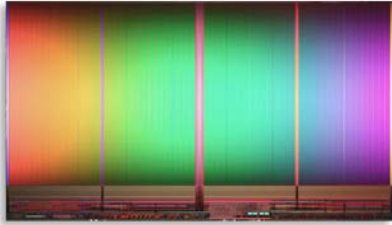
▪ Head to Tape (Media) Spacing

- Head structures recede (i.e. wear) from edges of closure and substrate during tape cycles
- This recession can be > 10 nm
(*A significant departure from HDD environment*)
- The tape media is thick > 50 nm
- Scaling to higher BPI densities requires reducing media thickness and reducing recession, i.e. Control of the head to tape spacing!!



Intel Micron 8 GB NAND Chip (2 bit per cell)

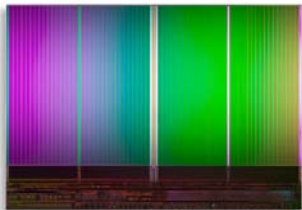
8 GB 25 nm IM Flash



16.5 mm

- **Chip Area** → 167 mm² (16.5 mm x 10.1 mm)
- **Active Memory Area** → 122 mm² (73% efficiency)
- **Minimum Feature (F)** → 25 nm
- **Memory Cell Area** → 1906 nm²
- **Memory Cell Area** → 3 F² (not 2 F² !!!)
- **Local Areal Density** → 330 Gb/in²

8 GB 20 nm IM Flash



- **Chip Area** → 118 mm² (12.5 mm x 9.5 mm)
- **Active Memory Area** → 71 mm² (63% efficiency)
- **Minimum Feature (F)** → 20 nm
- **Memory Cell Area** → 1109 nm²
- **Memory Cell Area** → 2.8 F² (not 2 F² !!!)
- **Local Areal Density** → 560 Gb/in²

NAND Landscape – Areal Density and Cost

- Use Intel Micron 8GB NAND device as a benchmark, assume \$1500 for 300 mm wafer processing

	2010	2011	2012-2013	2014 (?)
Device Capacity	8 GB	8 GB	16 GB	32 GB
Minimum F	25 nm	20 nm	16 nm	12.5 nm
Areal Density	330 Gbit/in ²	550 Gbit/in ²	660 Gbit/in ²	1330 Gbit/in ²
Devices / 300 mm Wafer	364	522	364	364
TB on 300 mm Wafer	2.9 TB	4.2 TB	5.8 TB	11.2 TB
\$ / GB at Wafer Level	\$0.52	\$0.36	\$0.26	\$0.13

- What could change? Transition to 3 bit per cell (8 voltage states) design. There is a reason why Intel Micron did not do this at the 25 nm node
- A comment \$/GB in this table
 - It is a “raw” component cost before sawing, thinning, packaging
 - A good HDD comparison is to use \$3 / head and \$3 / disk so a raw component cost to support a 1 TB platter is \$9 or **\$0.01 /GB**

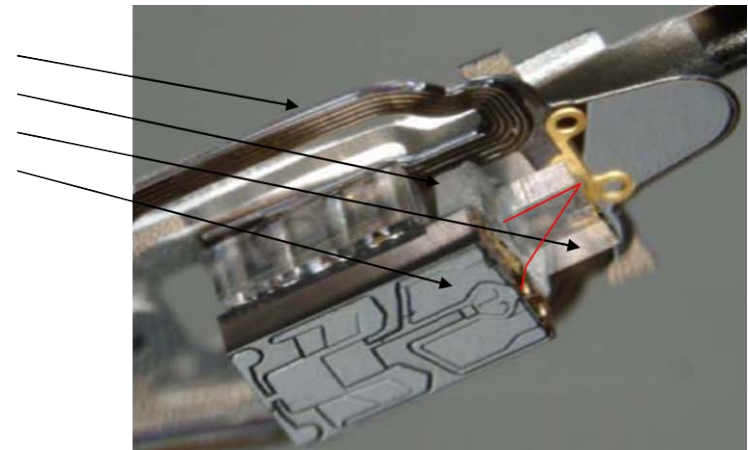
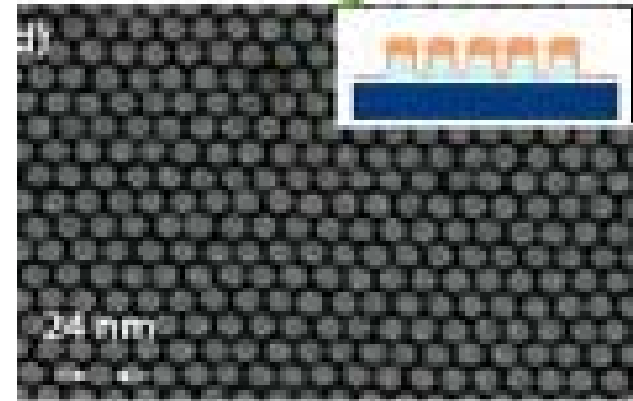
HDD Landscape – 750 GB Platter (3.5” disc, 2 surfaces)

- **Data storage capacity (GB) for a 3.5” platter ~ 1.2 (moving to 1.4) X Maximum Areal Density (Gb/in²) of the system → 635 Gbit/in² areal density supports 750 GB platter**
 - The “Maximum Areal Density” on the disk surface is at the inner tracks of a band
 - Surface area of a 3.5” platter ~ 17.5 in² → Average Areal Density on the platter is ~ 50% of the Maximum Areal Density
 - Overhead for edge exclusions, slider width, coding format,

- **750 GB platter details**
 - Areal Density (Maximum) → 635 Gbit/in²
 - Areal Density (Average) → 360 Gbit/in² (60% efficiency)
 - Memory Cell Area → 1000 nm²
 - Bit Aspect Ratio = 5.5 Scenario
 - Minimum Feature F → 37 nm (MR sensor width)
 - Memory Cell Area → 0.73 F²
 - MRw, Track Pitch, Bit Length → 37 nm, 74 nm, 13.5 nm
 - TPI, BPI → 338 KTPI, 1850 KBPI
 - Bit Aspect Ratio = 1.0 Scenario
 - Minimum Feature F → 16 nm (MR sensor width)
 - Memory Cell Area → 4.00 F²
 - MRw, Track Pitch, Bit Length → **16 nm**, 32 nm, 16 nm
 - TPI, BPI → 790 KTPI, 790 KBPI

HDD Landscape

- Continued 40% annual areal density increases will eventually require minimum features sizes for the MR sensor with smaller dimensions than semiconductor roadmap projections. Fortunately MR sensors are isolated structures.
- The decrease in bit aspect ratio (BAR) results in lithography driven areal density strategies, e.g. pattern media
- Media patterning strategies rely on introduction of imprint technology, a semiconductor roadmap strategy for 2014
 - E-beam lithography at 1X for master stencils
 - Patterning/Planarization/Stencil development and infrastructure → COST and TIME
- Energy assisted strategies must define trackwidths, ~ 2X MRw, using heat, by adding additional components onto the head slider
- Any new technology must be sustainable in the 2.5 Tbit/in² environment



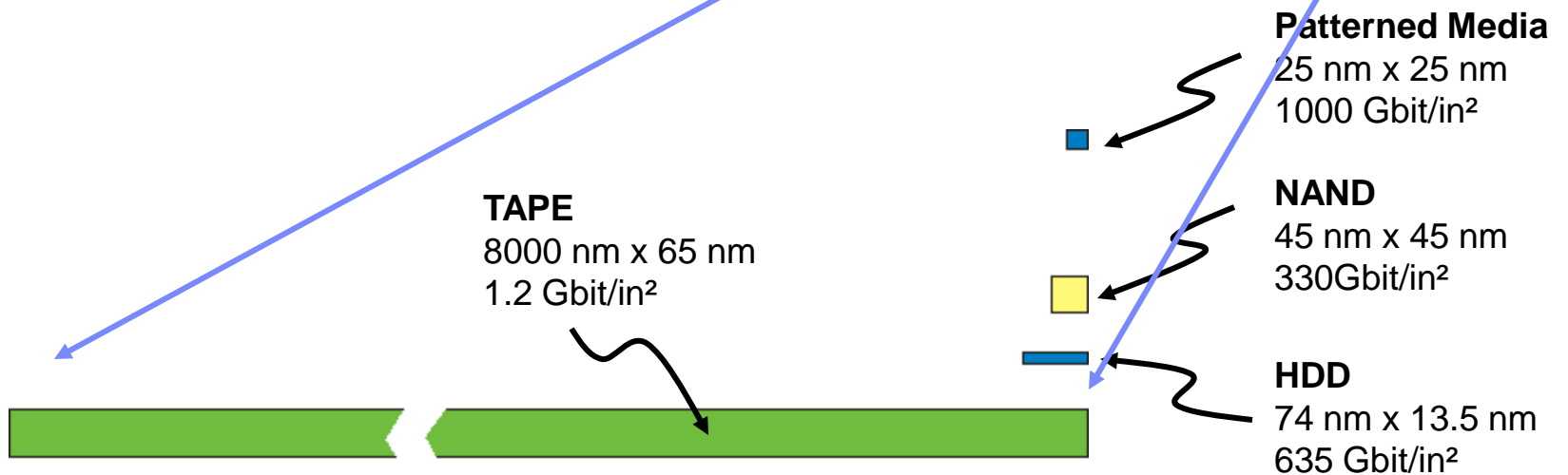
M. Re, "Has HAMR reached a critical mass", The Information Storage Industry Consortium Symposium on Alternative Storage Technologies, April 2009, www.insic.org

Storage Bit Cells and Extendability

- **Scaled Bit Cells**



- **Magnified View of Scaled Bit Cells**



Areal Density Scenarios relative to 2014

▪ HDD

- Conservative: 20% density increases achievable
- Aggressive: 30% density increases are challenging

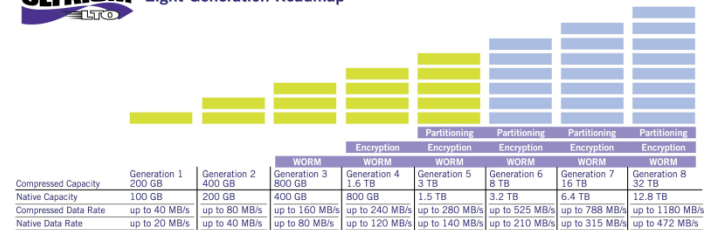
▪ NAND Flash

- Conservative: 20% density increases are achievable given the lithography roadmap strategies project reducing feature size 10% annually
- Aggressive: Sustained 30% density increases are difficult given the conventional understanding of lithography roadmaps and time driven optical processing tooling strategies. However, INTEL-MICRON has demonstrated a 40% areal density improvement from 2010 to 2011.

▪ TAPE

- Conservative: 40% density increases achievable with anticipation of following the LTO Roadmap presently at Generation 5
- Aggressive: 80% density increases are possible since the needed transducer technology presently exists in the HDD environment but “mechanical” issues related to positioning, wear, and tape stability must be addressed – not NANOSCALE issues

ULTRIUM LTO
Eight-Generation Roadmap



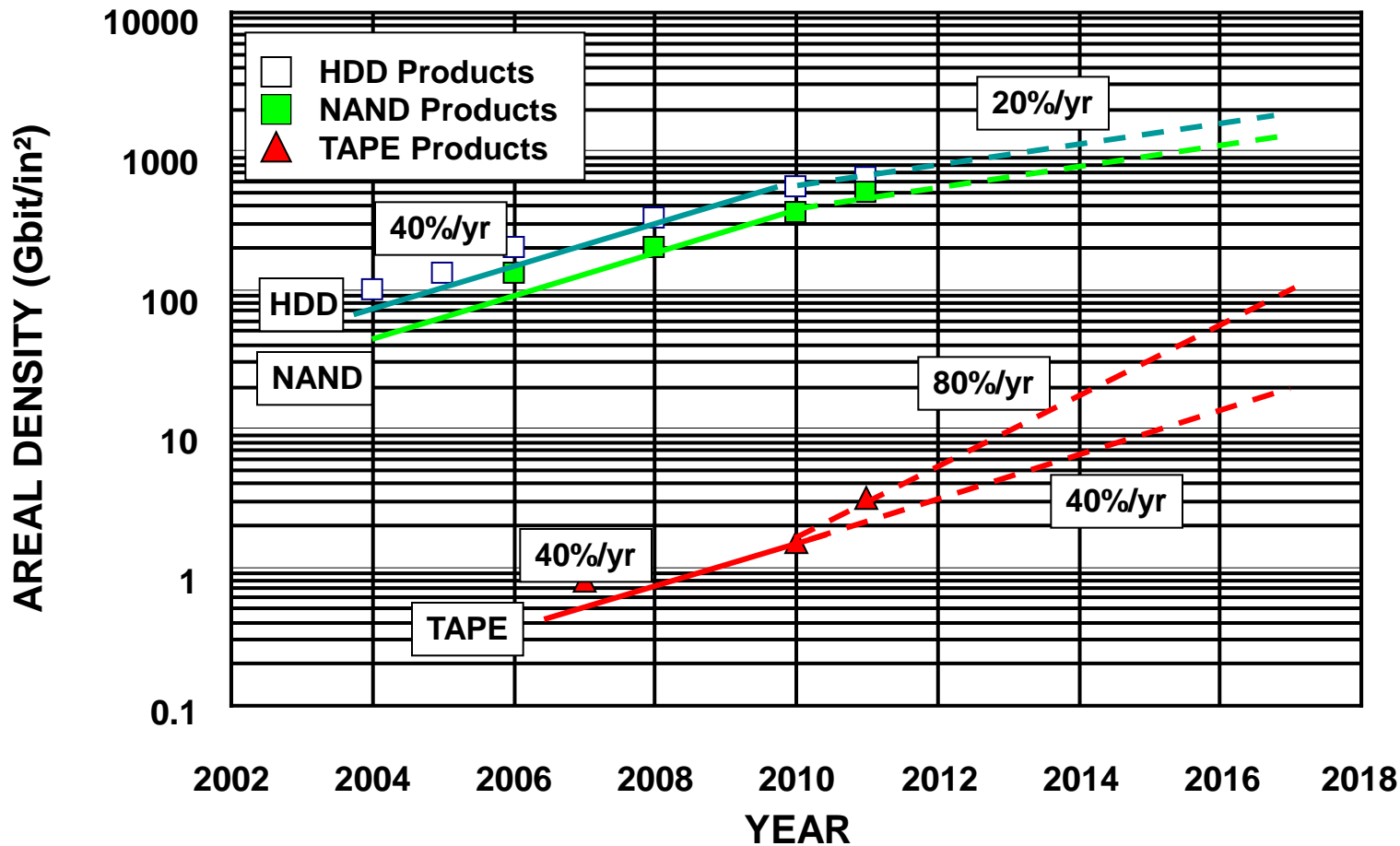
Note: Compressed capacities for generations 1-5 assume 2:1 compression. Compressed capacities for generations 6-8 assume 2.5:1 compression (achieved with larger compression history buffer).
Source: The LTO Program. The LTO Ultrium roadmap is subject to change without notice and represents goals and objectives only.
Linear Tape-Open, LTO, the LTO logo, Ultrium, and the Ultrium logo are registered trademarks of HP, IBM and Quantum in the US and other countries.

Scenarios for 2014

	Historical	Conservative	Tape Aggressive
Areal Density Growth (Specifics)	40%/yr--TAPE 40%/yr--HDD 40%/yr--NAND	40%/yr--TAPE 20%/yr--HDD 20%/yr--NAND	80%/yr--TAPE 20%/yr--HDD 20%/yr--NAND
<u>TAPE</u>			
-- Areal Density	4.8 Gbit/in ²	4.8 Gbit/in ²	12.0 Gbit/in ²
-- Minimum Feature	1.0 um	1.0 um	0.4 um
-- Cartridge Capacity	6.0 TB	6.0 TB	15.0 TB
-- Volumetric Density	404 GB/in ³	404 GB/in ³	1000 GB/in ³
<u>HDD</u>			
-- Areal Density	2500 Gbit/in ²	1300 Gbit/in ²	1300 Gbit/in ²
-- Minimum Feature	0.010 um	0.018 um	0.018 um
-- HDD Capacity ¹	12.0 TB	6.0 TB	6.0 TB
-- Volumetric Density	480 GB/in ³	240 GB/in ³	240 GB/in ³
<u>NAND Flash</u>			
-- Areal Density	1300 Gbit/in ²	700 Gbit/in ²	700 Gbit/in ²
-- Minimum Feature	0.012 um	0.016 um	0.016 um
-- Chip Capacity	32 GB	24 GB	24 GB
-- SSD Capacity ²	2 TB	1.2 TB	1.2 TB
-- Volumetric Density	480 GB/in ³	300 GB/in ³	300 GB/in ³

Annual Areal Density Growth Rate Scenarios

- HDD – 20% to 25% – Transition to New Technology, Sensor Output, Lithography
- NAND Flash – 25% to 30% – Lithography and Endurance
- TAPE – 40% to 80% -- No Lithography Issues, Mechanical Realities



Summary

- **Similarities: TAPE relative to NAND and HDD**
 - Device volumetric densities comparable in 1 TB capacity range
 - Areal efficiencies at the media surface area are comparable at ~ 65%
- **Differences: TAPE relative to NAND and HDD**
 - Area of bit cell ~200X larger, Media thickness ~200X thinner
 - Media is flexible → dimensional stability implications
 - No thermal kT fluctuations that impact endurance or bit cell stability
 - Lithography requirements not dependent on semiconductor roadmap innovations
- **Realities**
 - TAPE areal density increases will come from existing technology presently practiced by HDD, i.e. evolutionary.
 - HDD areal density increases will come from “revolutionary” technology
 - NAND areal density increases are driven by lithography (evolutionary), by multi bit cell designs (revolutionary).
- **Numbers**
 - Today’s lithographic features are **20 nm**; achieving **16 nm** is difficult for NAND and HDD
 - Areal Densities: HDD ~ **700 Gbit/in²**, NAND ~ **500 Gbit/in²**, TAPE ~ **2 Gbit/in²**
 - NAND cost is **10X** greater than HDD cost. HDD cost is **2.5X** greater than TAPE cost
 - Moore’s Law, i.e. capacity doubling per unit area every two years (**40% per year**), will change for NAND and TAPE

Storage Device Density Landscape – A Summary

- **HDD** → 20% to 25% annual density increases
- **NAND** → 25% to 30% annual density increases
- **TAPE** → 40% annual areal density increases; likely greater (80%??)

