Improving Min-sum LDPC Decoding Throughput by Exploiting Intra-cell Bit Error Characteristic in MLC NAND Flash Memory

Wenzhe Zhao[1], Hongbin Sun[1], Minjie Lv[1], ***Guiqiang Dong[2]****, Nanning Zheng[1], Tong Zhang[3]*

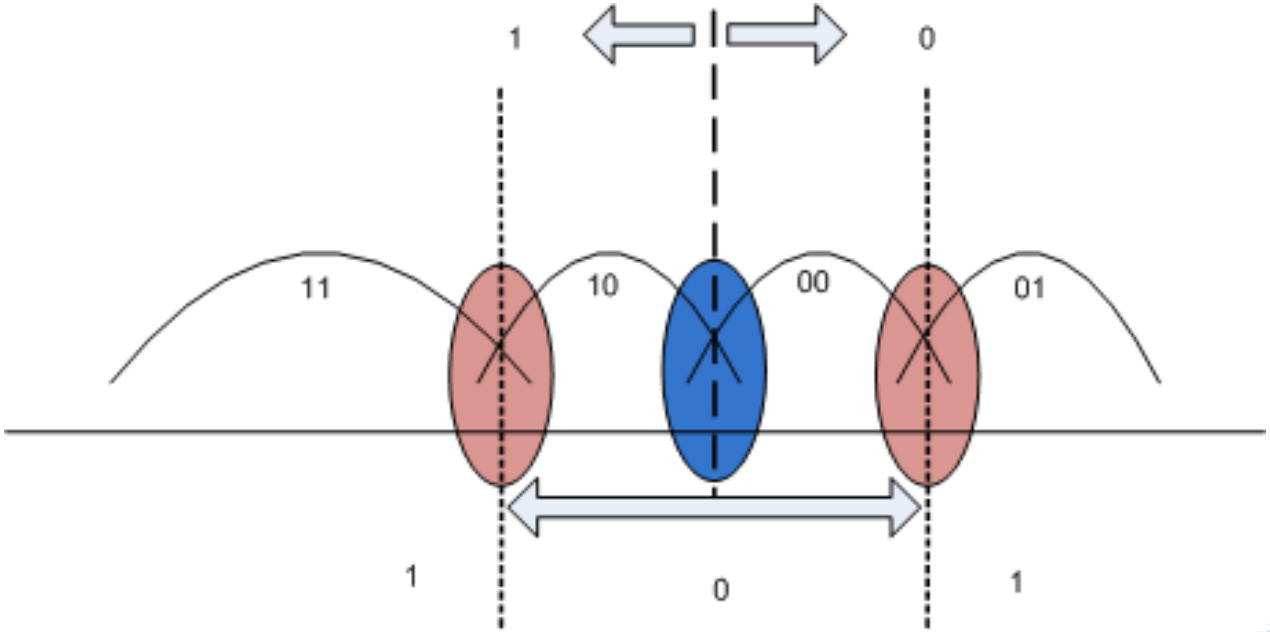
[1] Institute of AI&R, Xi'an Jiaotong University, Xi'an, Shaanxi, 710049, China

[2] Skyera Inc., 1704 Automation pkwy, San Jose, CA 95131, USA

[3] ECSE Department, Rensselaer Polytechnic Institute, Troy, NY, 12180, USA

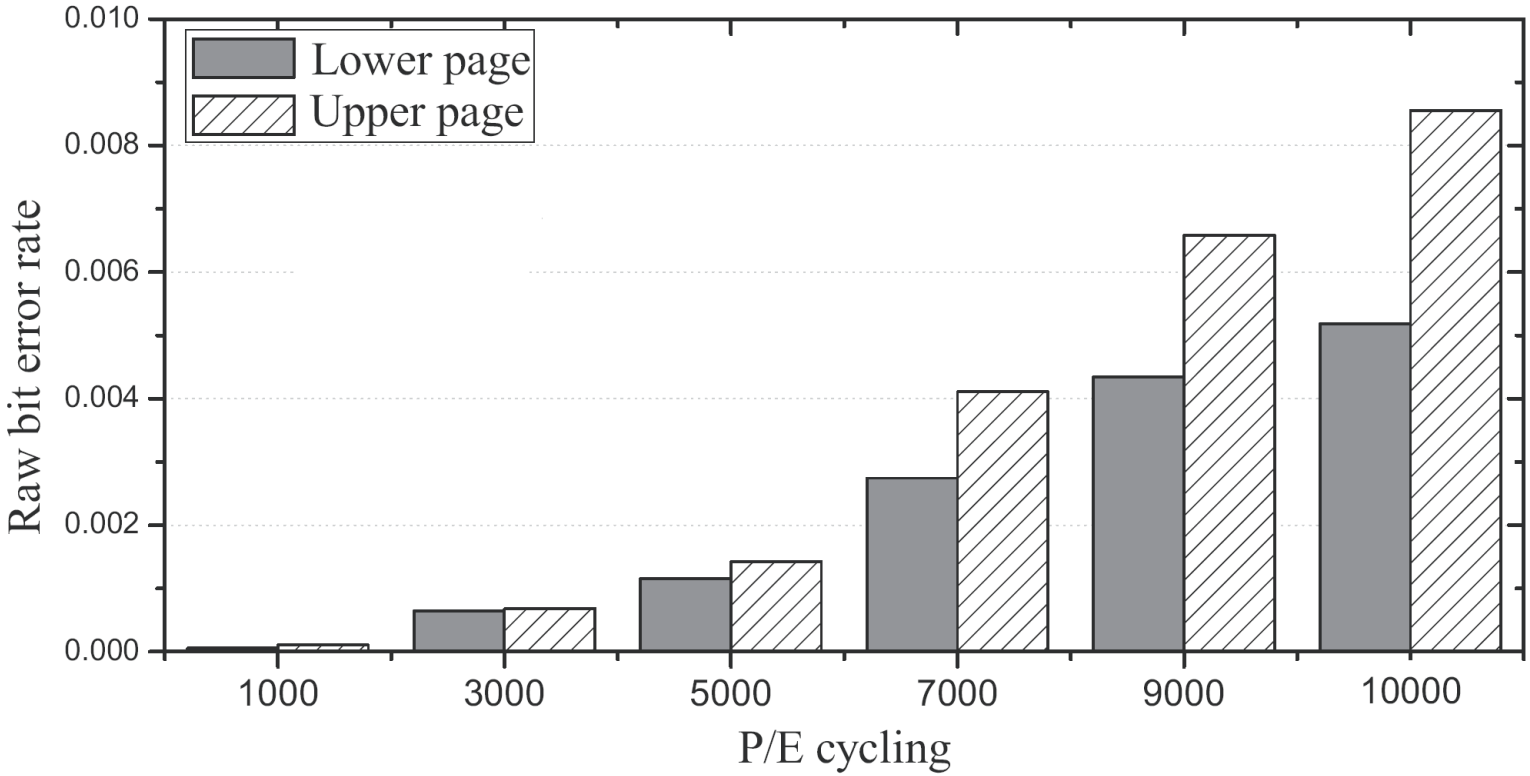
Observation 1

- In MLC/TLC NAND flash, error rates of bits in one cell are different.
- E.g.
- Lower page bit error <= one overlap
- Upper page bit error <= two overlaps ➔ 1 : 2



Test result

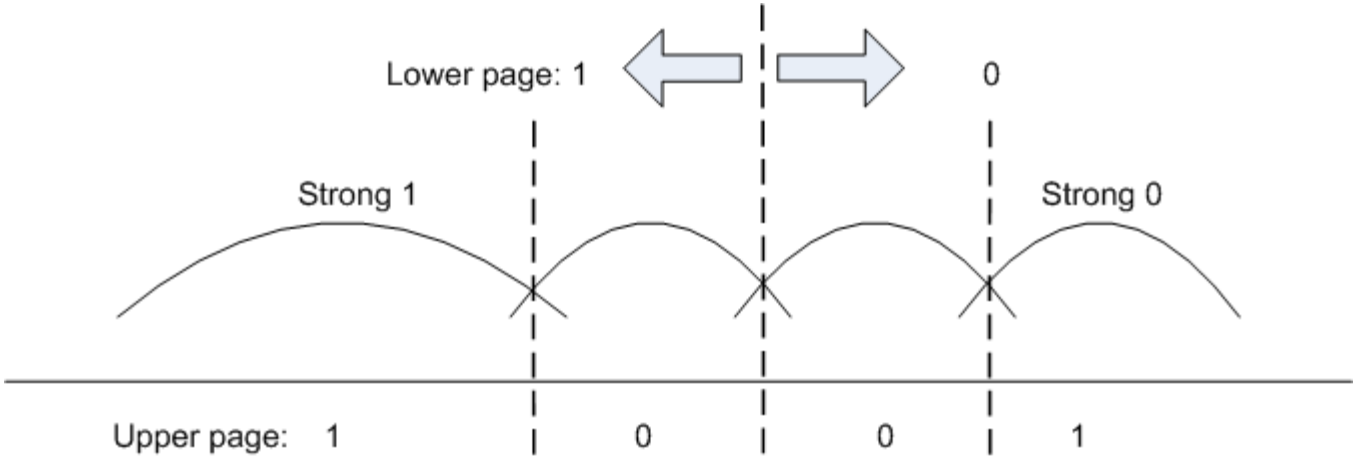
- Sub-22nm MLC NAND



Observation 2

- Under hard sensing in NAND flash cell, sensing results of one bit may provide EXTRA soft information (reliability infor) for the other bits

  => Inter-cell data dependency
- E.g. Upper bit can show to some extent the lower bit reliability



We propose to:

- 1: Map all bits in one cell into one codeword for LDPC code INTERLEAVING

  => reduce failure rate => reduce changes to trigger high-precision sensing => reduce latency and improve throughput.

- 2: Explore the inter-cell data dependency, and change Min-Sum decoder, to be aware of this data dependency.
- *The change on Min-Sum decoder: do some modification to C-to-V message, according to the neighbor bit values*

Step 3: Calculate the check-to-variable message $M_{j,i}$ each variable bit with $E_{j,i}$ and K_i, by

$$M_{j,i} = r_i + \sum_{j' \in A_i, j' \neq j} Ej', i + K_i,$$

Proposal

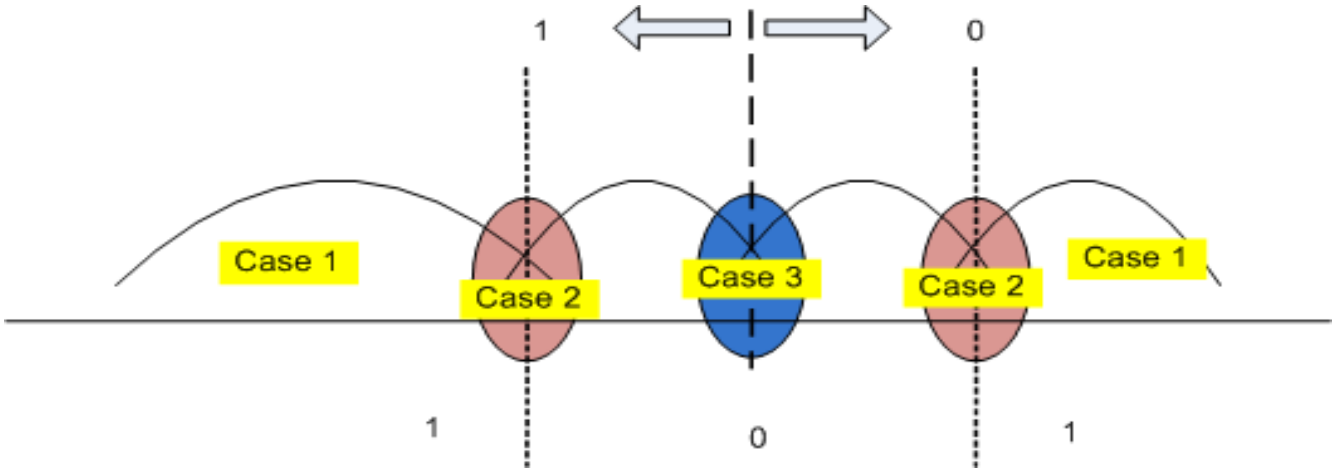
- Purpose of Ki: To enhance the reliability of the other bit.

$$K_i = \begin{cases} \alpha R_i & \text{if } R_c < 0 \&\& d_c < 0, i \in lower\ page \\ 0.5\alpha R_i & \text{else if } R_c d_c < 0, i \in lower\ page \\ 2 & \text{else if } R_c d_c < 0, i \in upper\ page \\ 0 & \text{else} \end{cases}$$

For bit in the same cell:

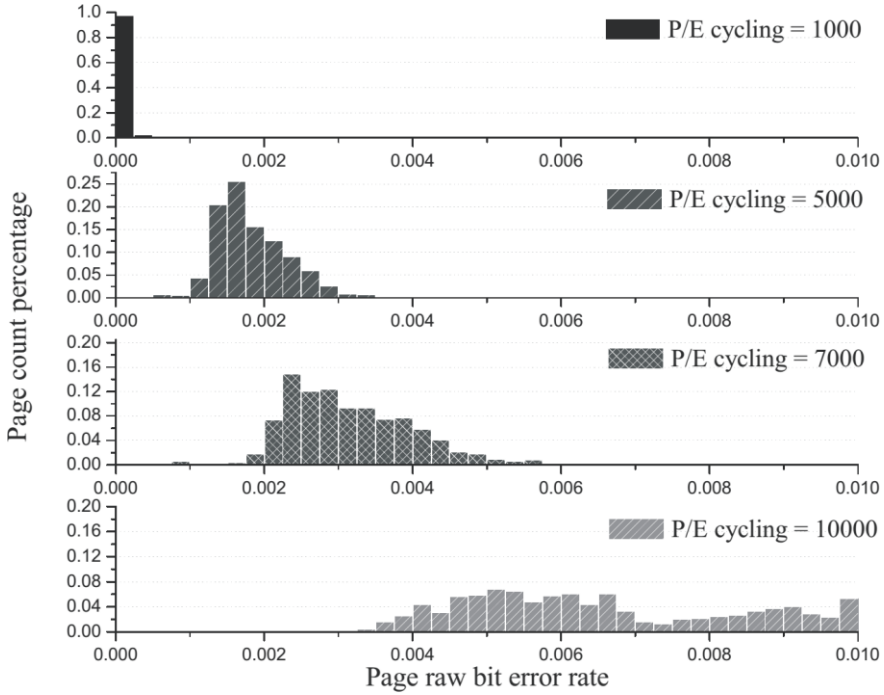
Rc: soft value from channel;

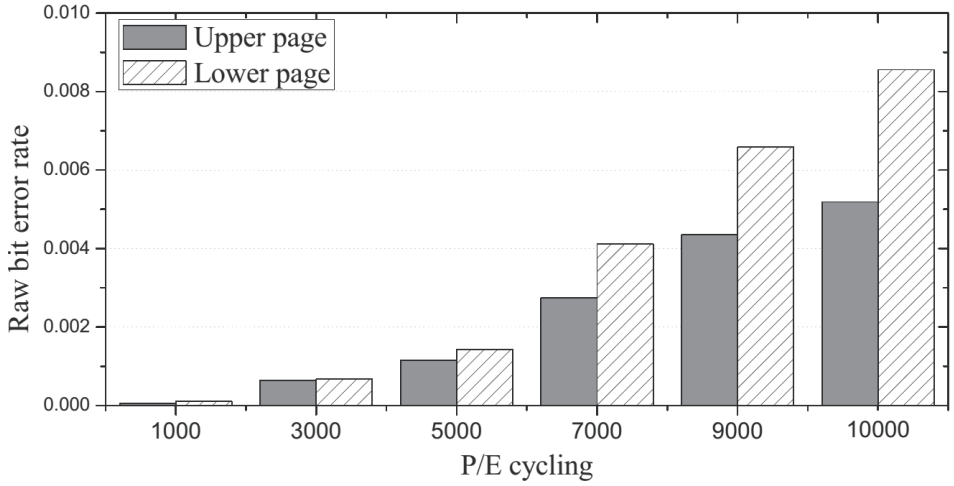
dc: sum of messages from all checks and channel => for hard decision.



Experimental Results

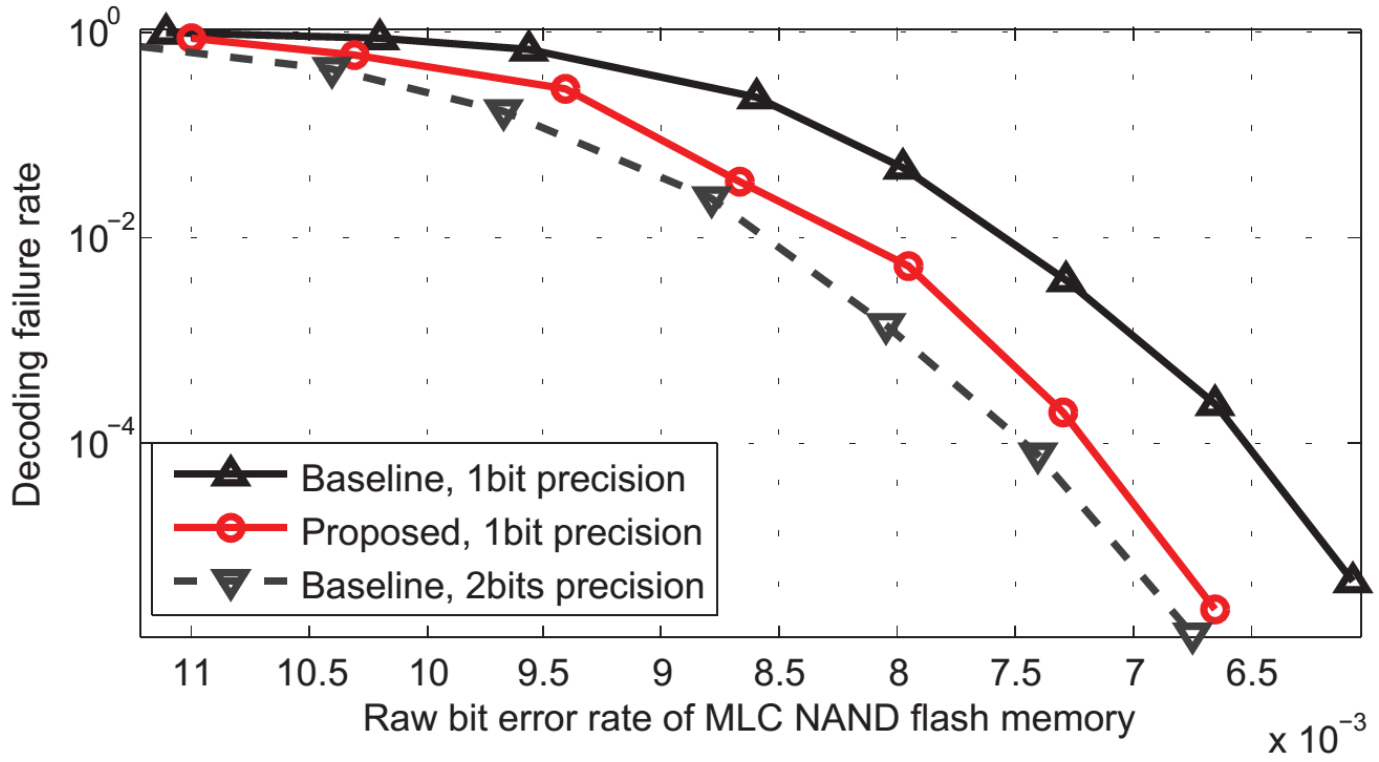
- Raw BER measurement of MLC NAND flash
  - With the increase of P/E cycling, flash reliability degrades
  - When flash is heavily cycled, BER of flash pages varies significantly
  - Upper/lower pages suffer different raw BER





Simulation Results

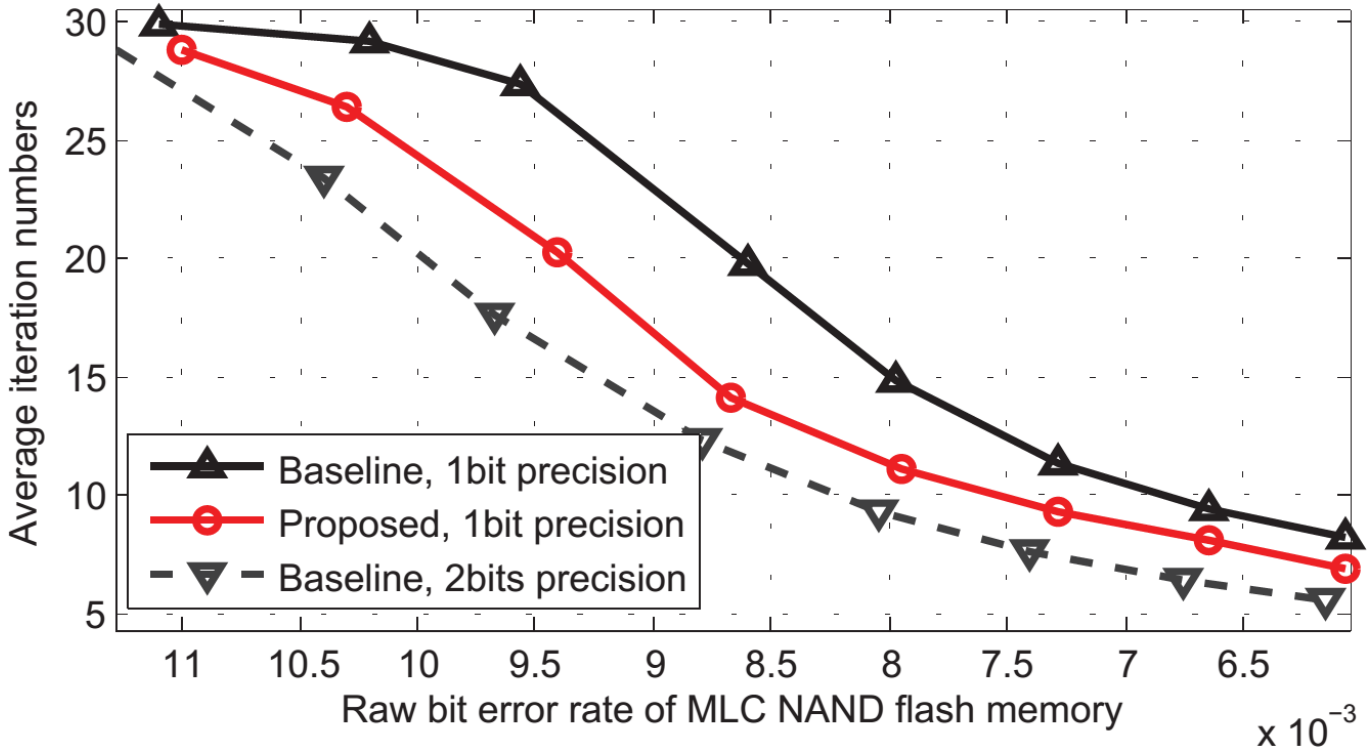
- Modified Min-Sum Decoding correction performance



  - The decoding failure rate of proposed algorithm is lower than before, and gets close to 2bits precision decoder

Simulation Results

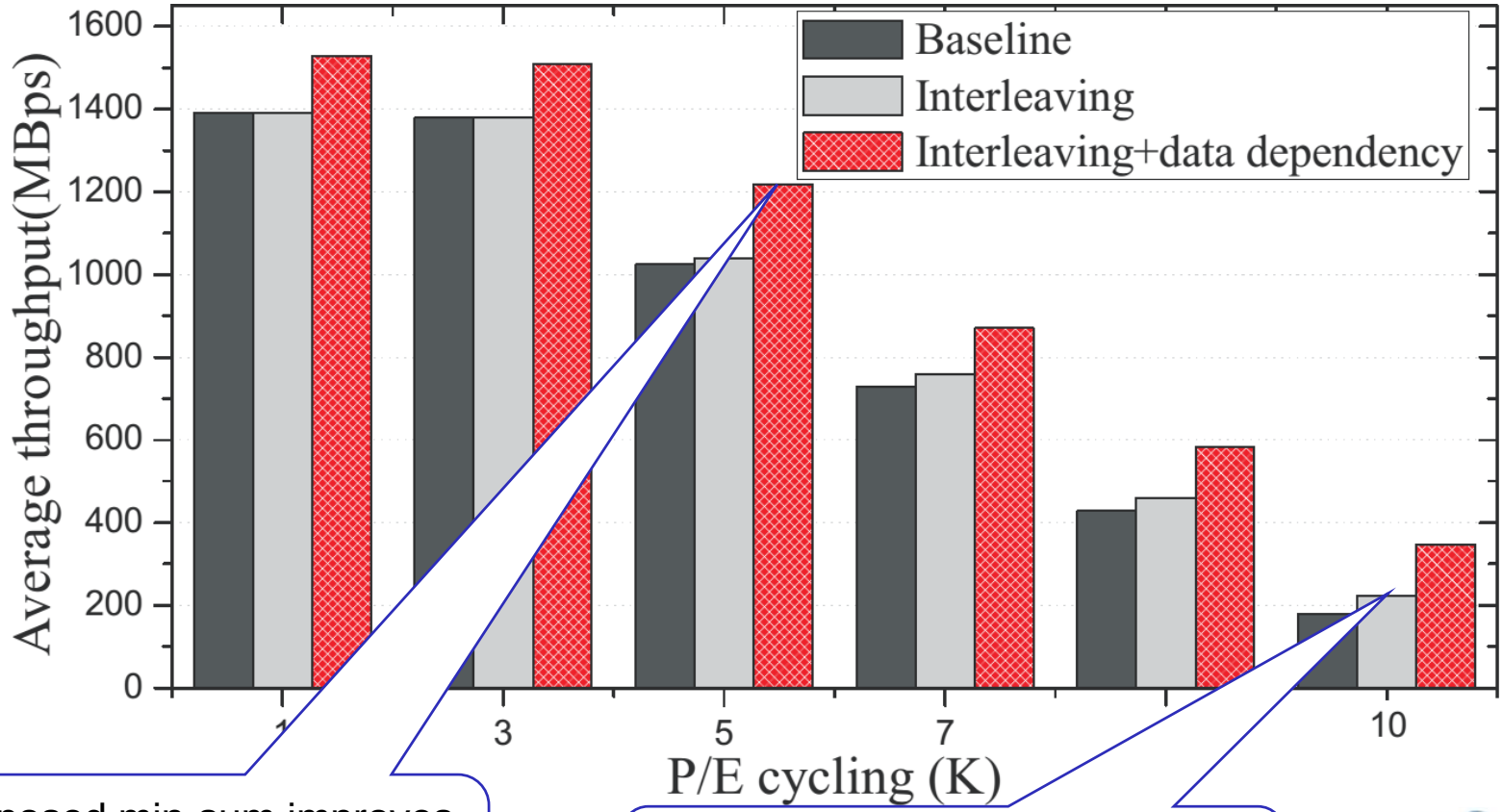
- Decoding convergence speed



  - The convergence speed of proposed algorithm is faster than conventional decoder

Simulation Results

- Estimated decoding throughput



Proposed min-sum improves throughput than conventional decoder

Interleaving improves throughput when flash is heavily cycled

Thanks for your attention