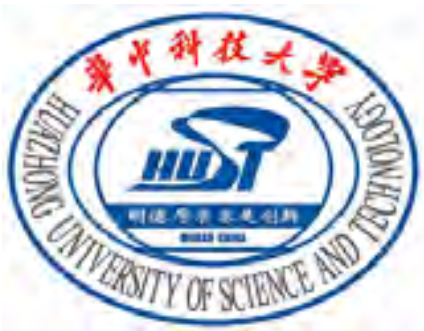
REAL: A Retention Error Aware LDPC Decoding Scheme to Improve NAND Flash Read Performance

Meng Zhang[*] Fei Wu[*] Xubin He[†] Ping Huang[†]
Shunzhuo Wang[*] Changsheng Xie[*]

[*]Wuhan National Laboratory for Optoelectronics,
Huazhong University of Science and Technology

[†]Department of Electrical and Computer Engineering,
Virginia Commonwealth University



May 5, 2016

Outline

NAND Flash and Issues Description

- **NAND flash** gains popularity in various markets.
  - High performance, low energy, small size
  - Increasing capacity, decreasing per-bit price

	SLC	MLC	TLC
Bits per cell	1	2	3
P/E Cycles	100,000	3,000	1,000
ECC capability	$\sim$ 4	$\sim$ 24	$\sim$ more

Source: White Paper "Solid State Drive Technology" from HP, 2013.

- **Results**
  - Storage density **increases**
  - Lifetime and data reliability **reduces**

Program/Erase (P/E) Cycles and Retention Error[1]

- **P/E cycles and retention error (domain error) influences on data reliability**:

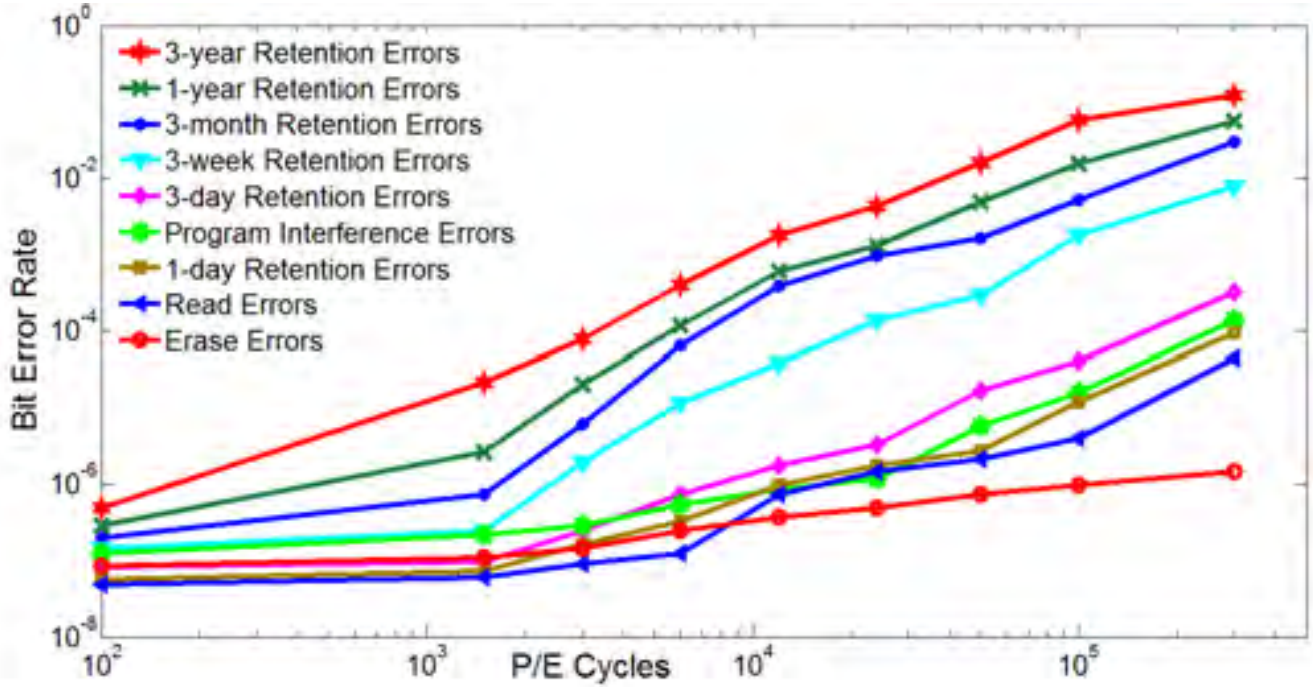


Figure: Rates of various types of errors as P/E cycles

- P/E cycles **increase**, retention time **long**, data reliability **decreases**

[1]Figure Source: Cai et al [2] DATE 2012

Error correcti

- To ensure c
  - BCH (r
  - Low de

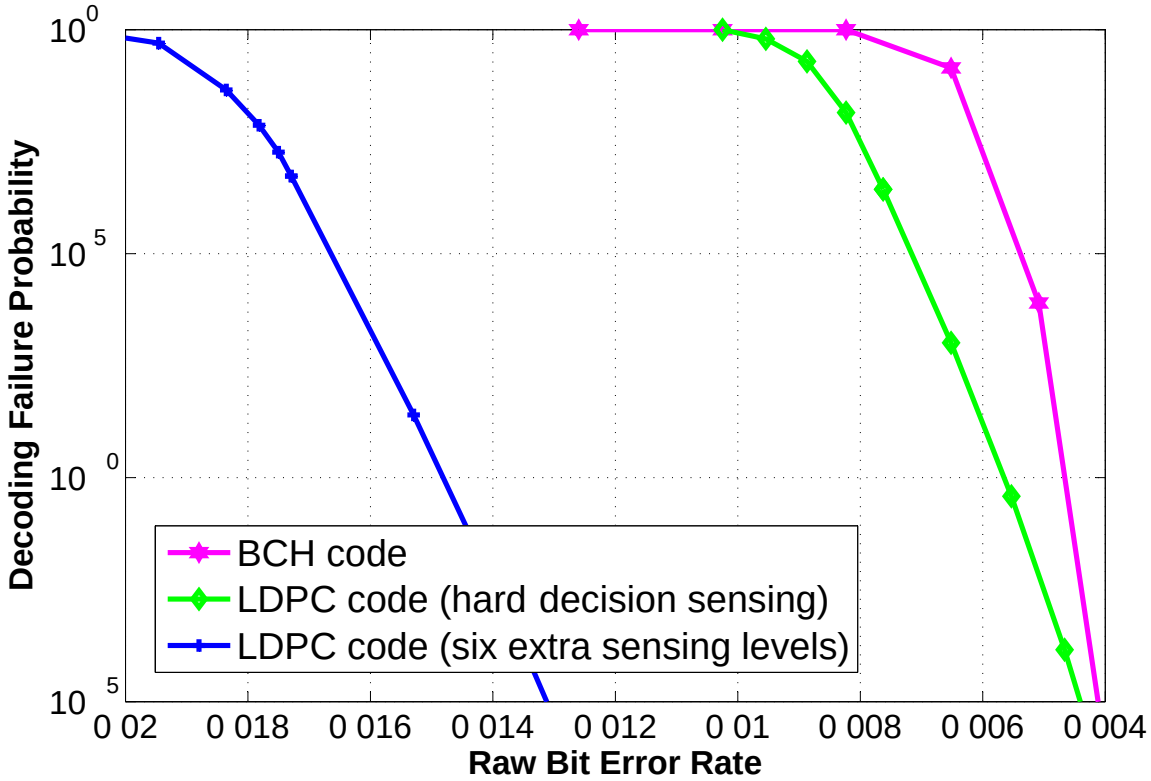


Figure: Decoding performance comparison

[2]Figure Source: Zhao et al [3] FAST 2013

LDPC [3]

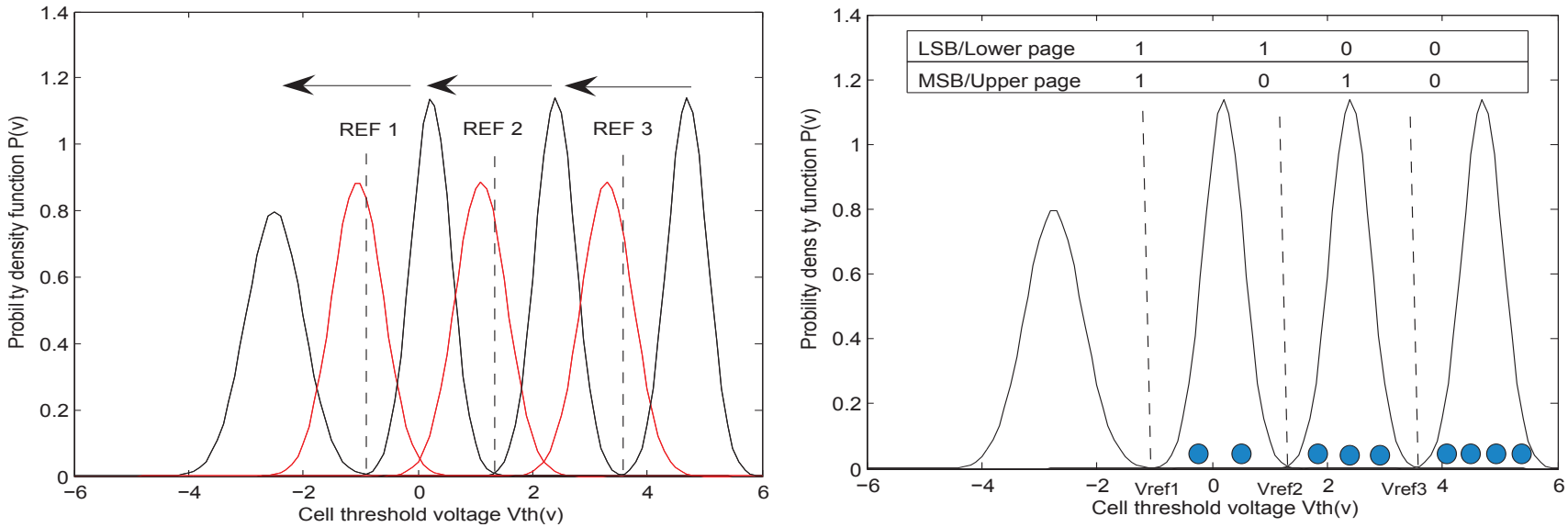
- Directly using LDPC (without optimization, high compexity) introduces non-trivial overhead
  - (a) Decoding latency increases
  - (b) NAND flash read performance degrades
- How to solve the issue?
  - (a) Optimization LDPC
  - (b) Reduce decoding latency and improve NAND flash read performance

[3] References: Zhao et al [5] MSST 2014

Outline

Retention Error Characteristic

- **Charges leakage** (theshold voltage shifts)



(a) Theshold voltage shifts (red line) (b) Mapping information bits to voltage

- **Numerical correlation** $\rightarrow$ Two bits from the same cell affect each other with charges leakage.

00$\rightarrow$01	01$\rightarrow$10	01 $\rightarrow$11	10$\rightarrow$11
46%	**44%**	5%	2%

Source: Cai et al [2] DATE 2012

REAL

- We propose **REAL** scheme
  - to incorporate the numerical-correlation of retention errors into the process of LDPC decoding
  - to provide additional bits desicion information
  - to reduce decoding latency and improve NAND flash read performance

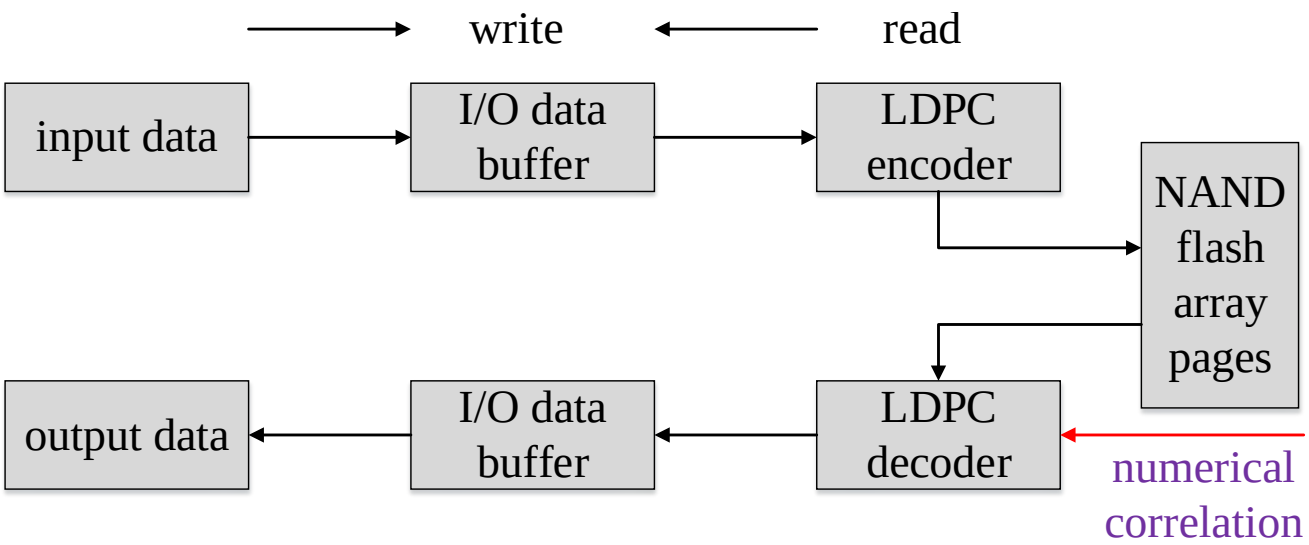


Figure: Numerical correlation is integrated into the decoding process.

How to use the numerical correlation?[4]

- make full use of the numerical correlation?

  (1) adjust LDPC codewords layout

  (2) obtain several observations based on the numerical correlation

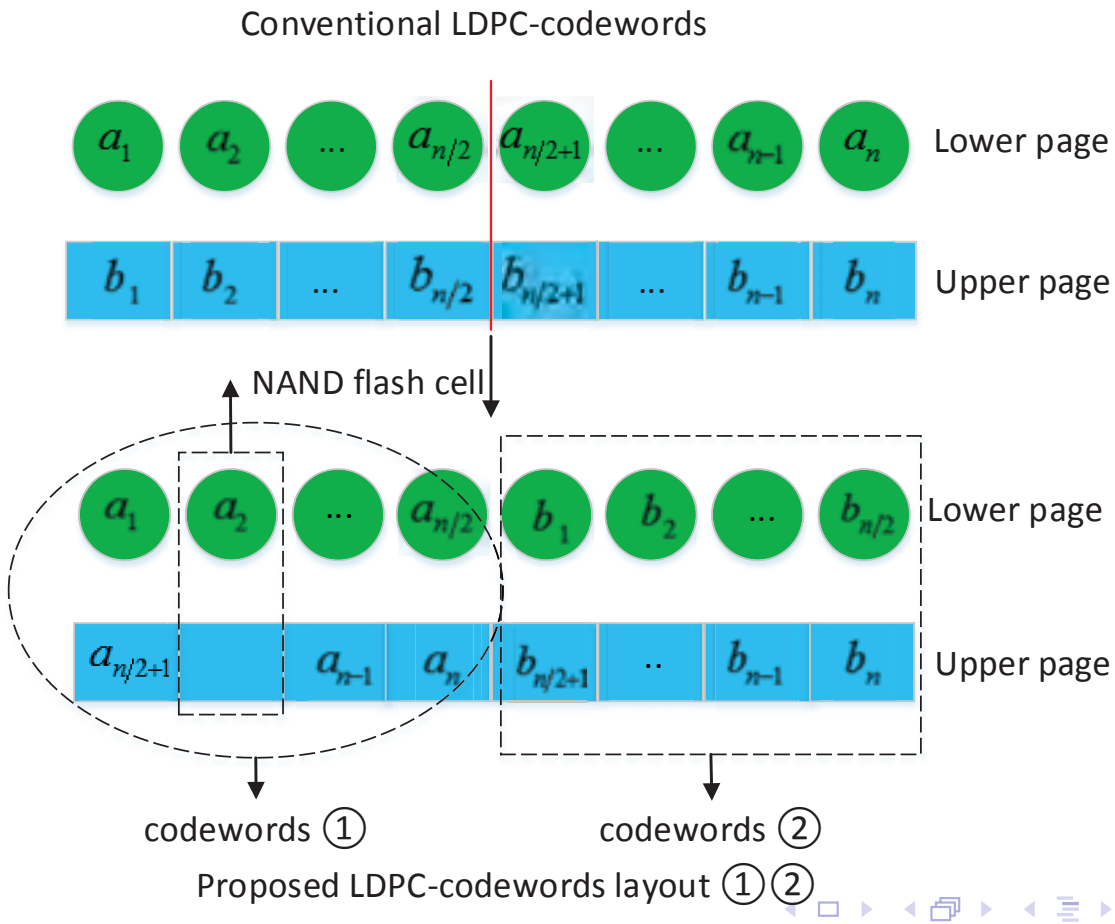
  (3) translate these observations into mathematical models

  (4) the translated mathematical models are added into the decoding process.

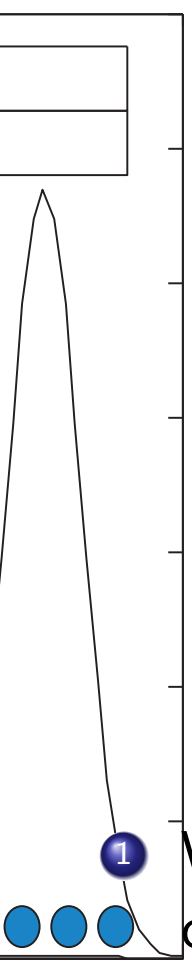
[4] Specific details can be found in our paper

LDPC Codewords Layout

1. to make a codeword contains two bits from the same MLC NAND flash cell
2. to provide the chance and environment that can effectively utilize the numerical correlation characteristic for the proposed REAL scheme



Our Observations [5]



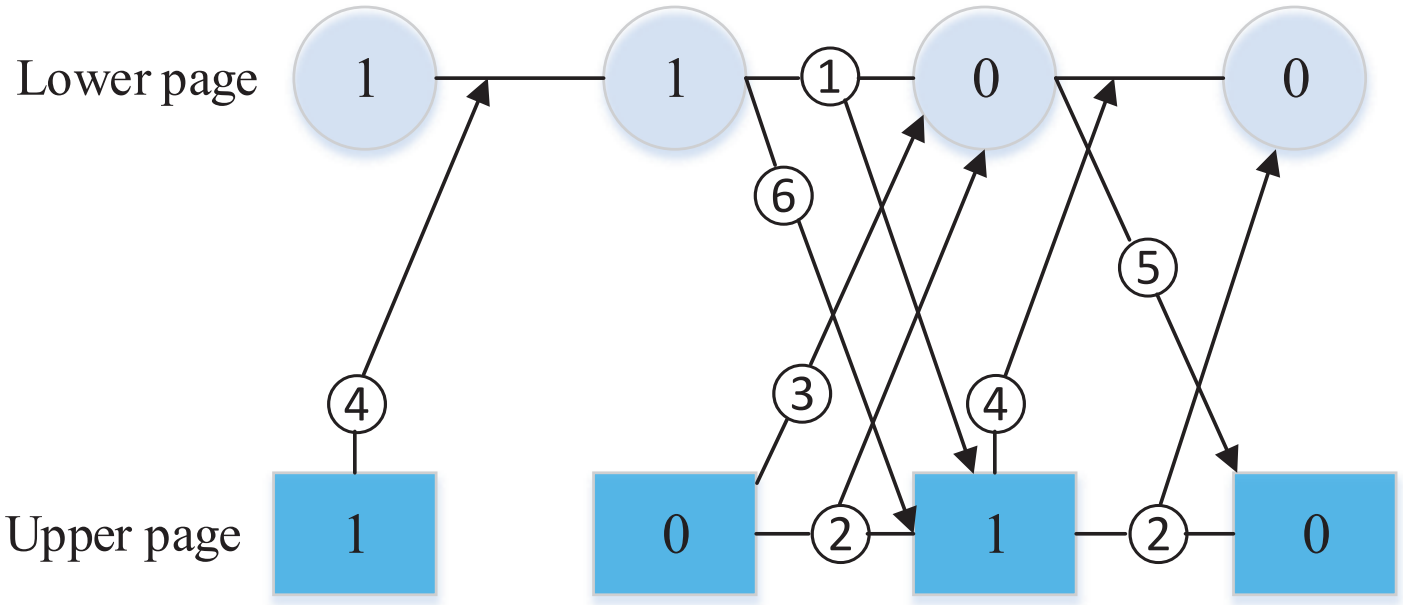


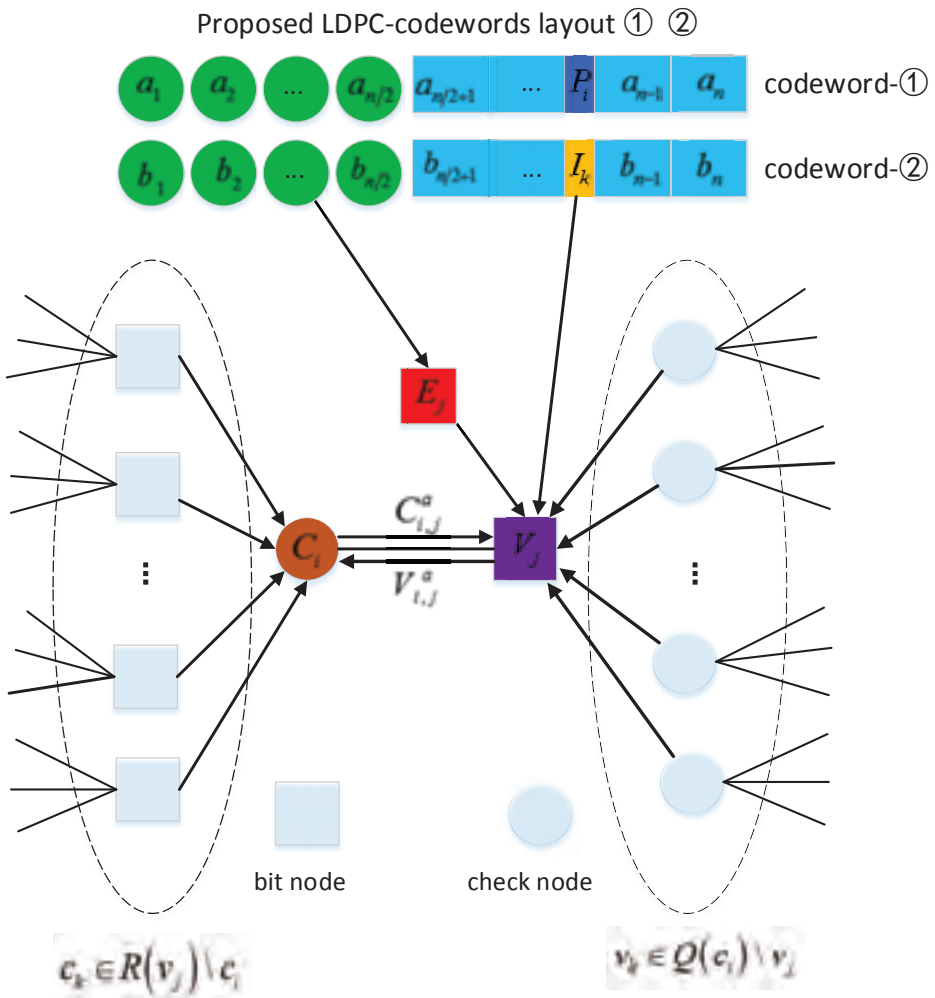
Figure: Observation overview.

1. We obtain several valuable observations based on the numerical correlation characteristic of retention errors (**MLC NAND flash**)

2. Symbols ① ② ③ ④ ⑤ ⑥ correspond to the 6 observations respectively.

[5] More details can be found in our paper

Work Process[6]



- When decoding, the additional decoding information E_j is provided

[6] The translated mathematical models can be found in our paper

Outline

Evaluation Methodology

- Simulation
  - build MATLAB simulation environment
  - utilize the AWGN (Additive White Gaussian Noise) channel to simulate the flash channel
- LDPC configuration

Codeword Length	(256×9)B
Information Length (Page Size)	2KB
Column Weight	4
Row Weight	36
Code Rate	8/9

- Experiment steps
  - construct the check matrix
  - information bits are encoded by applying the Gauss elimination algorithm
  - adding simulated retention error noise and decoding

Evaluation Results (Decoding Iterations)

(a) Decoding iterations comparison: Probability Domain BP (PD-BP), Logarithm Domain Min-Sum (LD-MS) and **REAL**

(b) SP/SNP represents signal power to retention noise power ratio

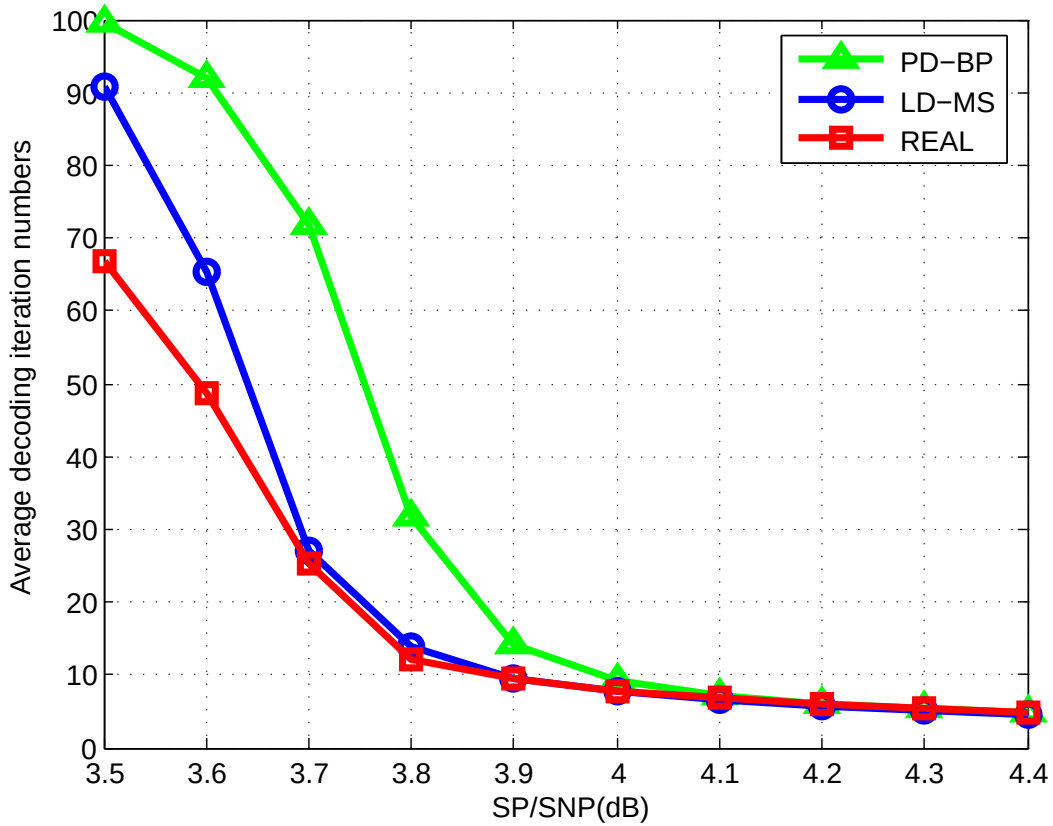


Figure: Comparison of decoding iterations at different SP/SNP

Decoding Failure Rate

(1) The failure rate of the decoded codewords is lower than the baselines
(2) If the SP/SNP continues decreasing, the baselines are not able to correct the LDPC codewords (REAL can be competent)

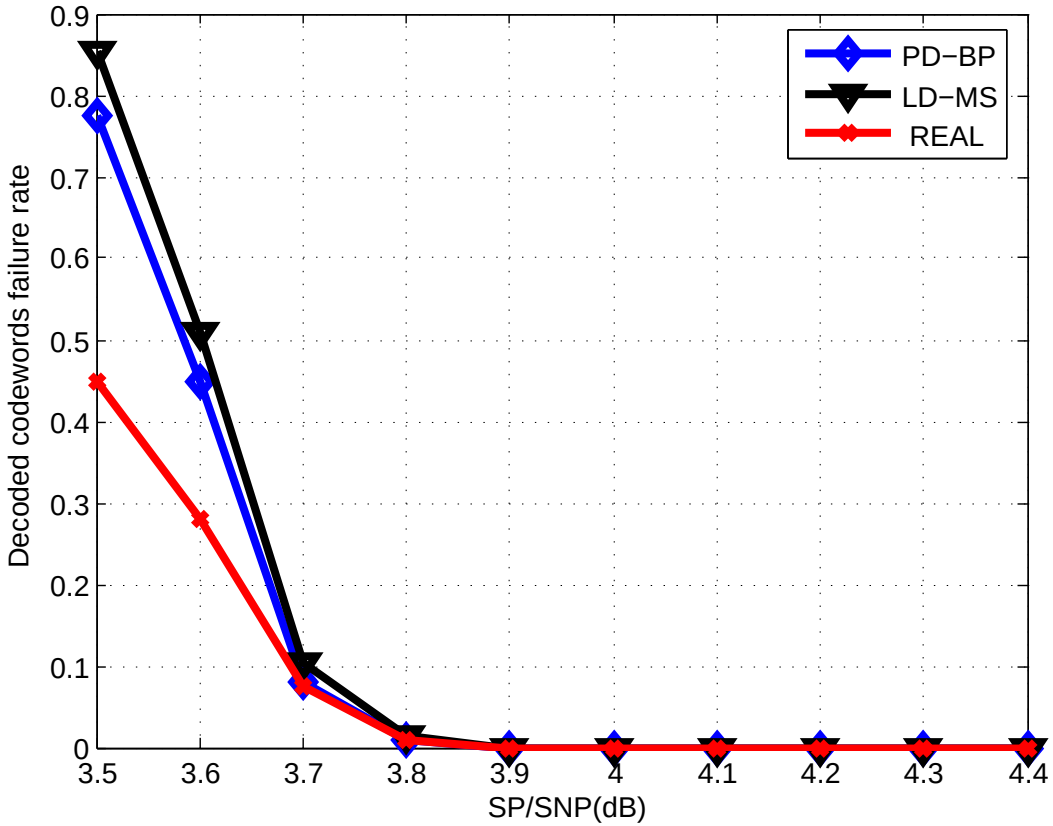
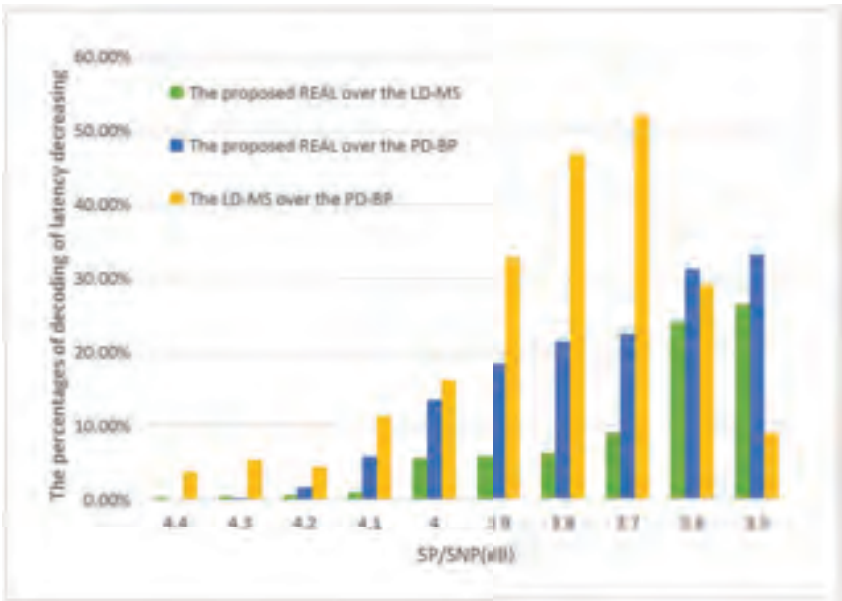


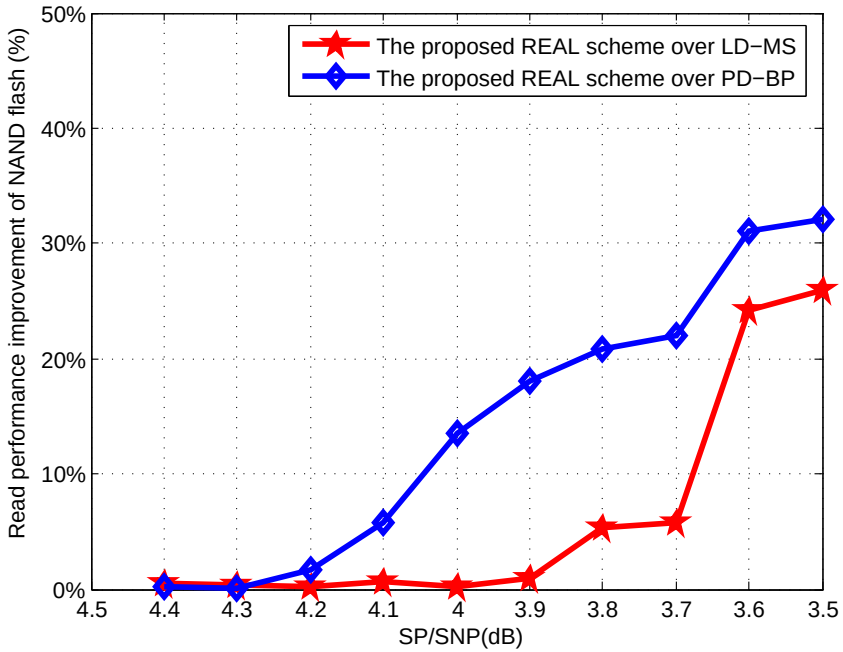
Figure: Comparison of decoding iterations at different SP/SNP

Decoding Latency and Read Performance of NAND Flash

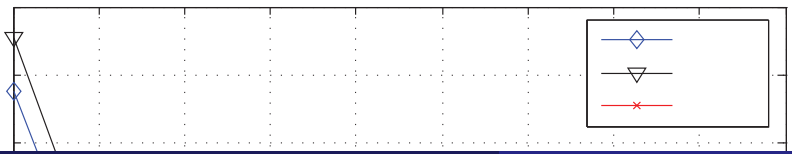
- REAL reduces decoding latency by 26.44% and 33.05%.
- REAL improves NAND flash read performance.



(a) The reduced decoding latency with REAL.



(b) The improvement in NAND flash read performance of our scheme.



Outline

Conclusion

- In order to reduce the influences of NAND flash retention errors and improve the stored information reliability, we adopt the LDPC codes with optimized decoding performance.
- Retention errors of NAND flash cells have the characteristic of numerical-correlation that motivates us to effectively leverage the characteristic in the process of LDPC decoding in order to decrease the decoding latency and thus improve the NAND flash read performance.
- we propose the REAL scheme that accounts for the numerical-correlation characteristic into the LDPC decoding process, which can reduce the LDPC decoding latency and improve the read performance of NAND flash.

Acknowledgement

- **We would like to thank Xiaosong Ma, our shepherd, and the anonymous reviewers for their valuable comments that greatly improved our paper.**

- This research is sponsored by the National Natural Science Foundation of China, National Natural Science Foundation of Hubei Province, the Education Ministry of Hubei Province of China, the National High Technology Research and Development Program of China (863 Program), Key Laboratory of Data Storage System, and U.S. National Science Foundation.

The End

Thanks !