Hibachi: A Cooperative Hybrid Cache with NVRAM and DRAM for Storage Arrays

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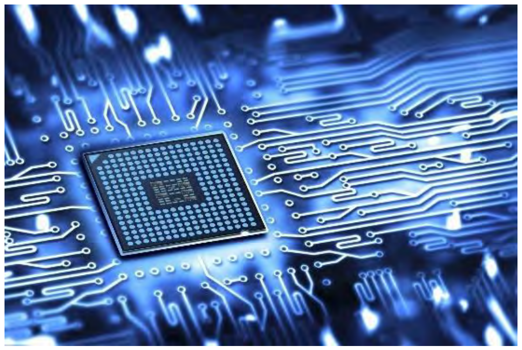
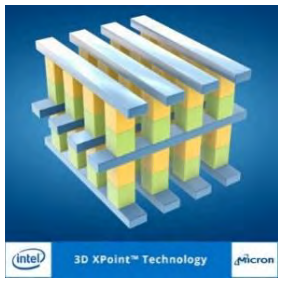
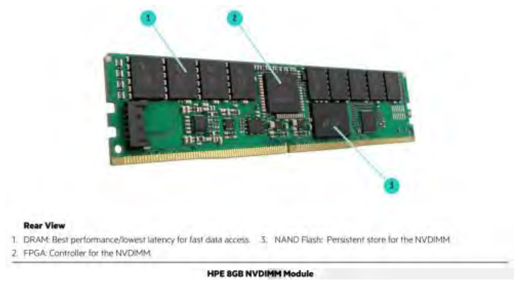
Hardware evolution leads to software and system innovation!



The hardware evolution of non-volatile memory (NVRAM)



3D Xpoint
(By Intel and Micron)


1
2
3
Rear View
1. DRAM: Best performance/lowest latency for fast data access.
2. FPGA: Controller for the NVDIMM
3. NAND Flash: Persistent store for the NVDIMM
HPE 8GB NVDIMM Module

NVDIMM
(By HPE)

STT-MRAM
(By Everspin)

- ✓ Non-volatile
- ✓ Low power consumption
- ✓ Fast (close to DRAM)
- ✓ Byte addressable
- ✓ …

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How to innovate our software and system to exploit NVRAM technologies?

Many Possible Ways

Caching Systems

Application Upgrade

OS Optimization

Design NVRAM-based caching systems to improve storage performance

Research Contributions

Extend **solid state drive** lifespan

→ H-ARC (in MSST 2014 [1]) 1

→ WRB (under TOS Major Revision) 2

Increase **hard disk drive** I/O throughput

→ I/O-Cache (in MASCOTS 2015 [2]) 3

Improve **disk array** performance

→ Hibachi (in MSST 2017 [3]) 4

Parallel File System

Increase **PFS** checkpointing speed

→ CDBB (Under Submission) 5

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A Cooperative Hybrid Cache with NVRAM and DRAM for Disk Arrays

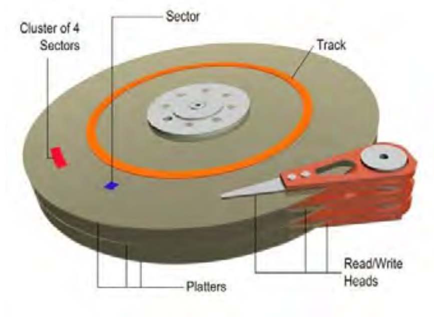
Outline

- Motivation
- Related Work
- Design Challenges
- **Our Approach**
- Evaluation
- Conclusion

Introduction

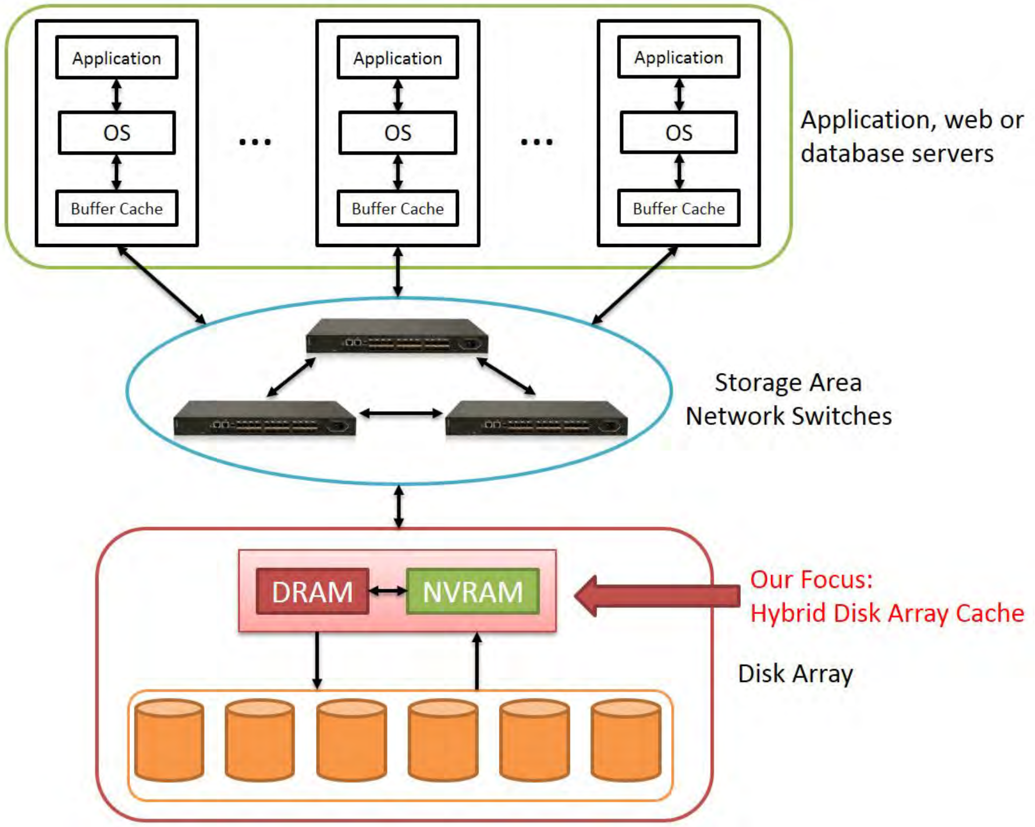
- Despite the rise of SSDs, disk arrays are still the backbone storage, especially for large data centers
- HDDs are much cheaper in capacity/$ and do not wear out easily

- However, as rotational devices
  - HDDs sequential throughput: ~100MB/s
  - HDDs random throughput : < 1MB/s



[4]

Introduction



- To improve disk performance, we use NVRAM and DRAM as caching devices
  - Disk cache is much larger than page cache and DRAM is more cost-effective than NVRAM
  - DRAM has lower latency than some types of NVRAM

Crux: How to design a hybrid disk cache to fully utilize scarce NVRAM and DRAM resources?

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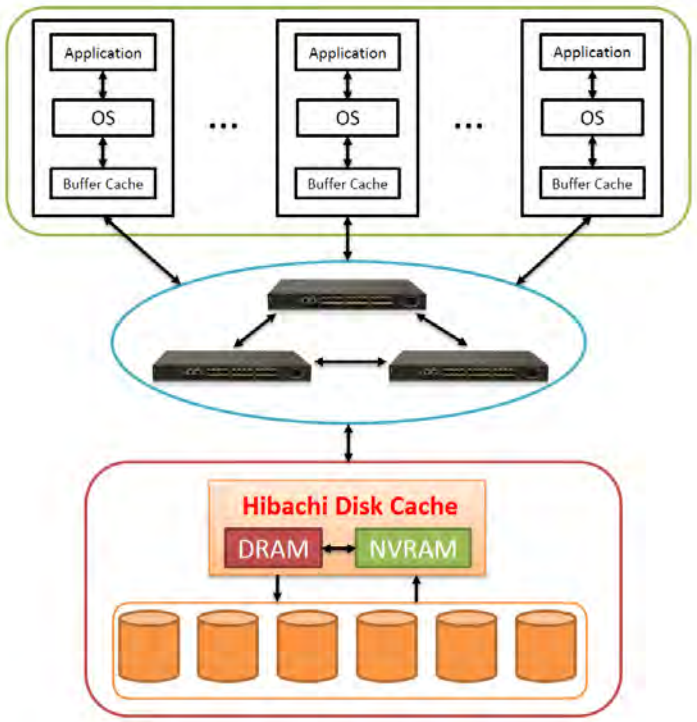
Related Work

- Cache policies designed for main memory (first-level cache)
  - **Not directly applicable to disk cache**
  - LRU, ARC[5], H-ARC [1]
- Multilevel buffer cache (including both first-level and second-level caches)
  - **Concentrate on improving read performance**
  - **Not considering NVRAM**
  - MQ [6], Karma [7]
- Disk cache with DRAM and NVRAM
  - **DRAM as read cache and NVRAM as write buffer $\rightarrow$ lack cooperation**

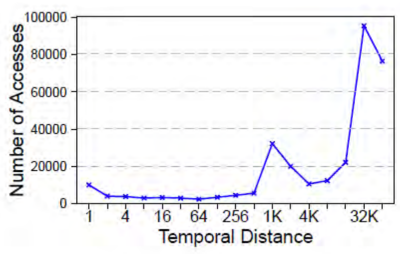
Design Challenges

- How to analyze and utilize I/O traces after first-level cache to design disk cache as second-level cache?
- How to utilize DRAM to maximize read performance?
  - Low access latency (high cache hit rate)
- How to utilize NVRAM to maximize write performance?
  - High I/O throughput
- How to exploit the synergy of both NVRAM and DRAM?
  - Help each other out according to workload properties

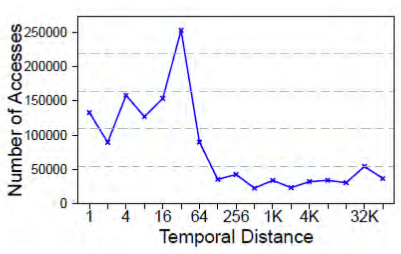


I/O Workload Characterization of Traces after First-level Cache

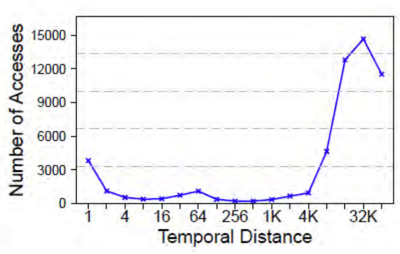
- Existing work only characterizes read requests [10]
- On top of existing work, we characterize both read and write requests



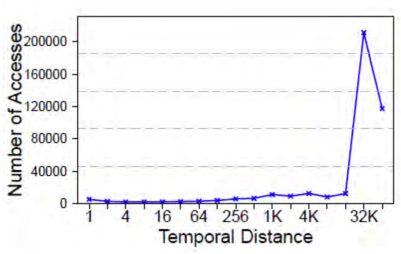
(a) web_0 read after read



(b) web_0 write after write



(c) web_0 read after write



(d) web_0 write after read

Temporal distance histograms of a storage server I/O workload.

✓ For read requests, stack distance is large -> recency is bad

✓ For write requests, stack distance is relatively short -> recency can be useful for cache design

✓ Frequency is useful for both read and write

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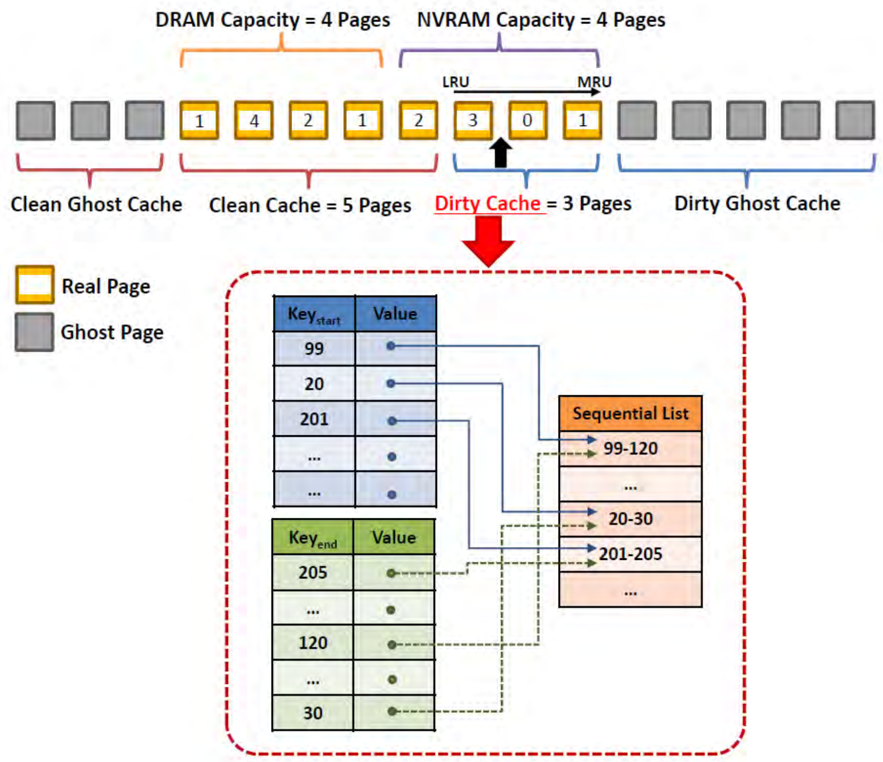
Hibachi – Cooperative Hybrid Disk Cache

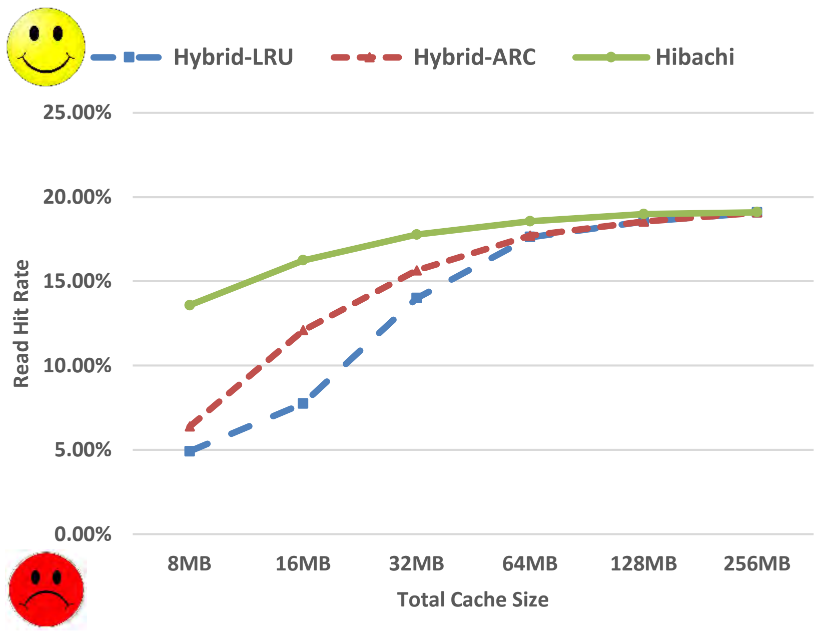


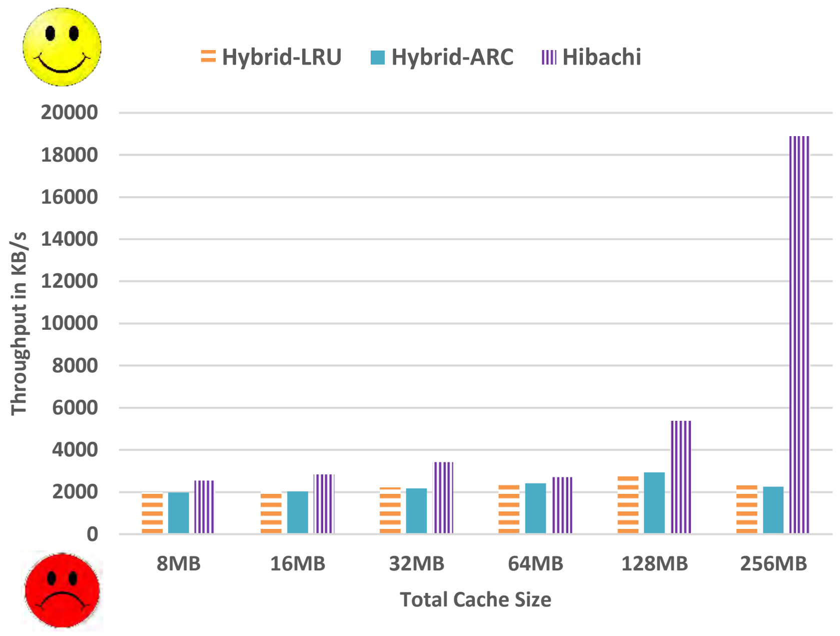
- Our Hibachi's **four** secret ingredients to make it "taste better"
  - Right Prediction → Improve cache hit ratio
  - Right Reaction → Minimize write traffic and increase read performance
  - Right Adjustment → Adaptive to workload
  - Right Transformation → Improve I/O throughput

Evaluation Setup

- Use Sim-ideal [9] to measure read performance
- Use software RAID with six disk drives to measure write performance
- Comparison algorithms:
  - Hybrid-LRU: DRAM is a clean cache for clean pages, and NVRAM is a write buffer for dirty pages. Both caches use the LRU policy.
  - Hybrid-ARC: An ARC-like algorithm to dynamically split NVRAM to cache both clean pages and dirty pages, while DRAM is a clean cache for clean pages.

Evaluation Results





- Hibachi outperforms Hybrid-LRU and Hybrid-ARC in
  - Read hit ratio
  - Write hit ratio
  - I/O throughput

Conclusion

- NVRAM as caching is a challenging and rewarding research topic
- We design Hibachi – a hybrid NVRAM and DRAM cache for disk arrays
  - Characterize storage-level workload to get design guidance
  - Our four features make Hibachi standing out
- Hibachi outperforms existing work in both read and write

References (1/2)

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Questions?

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