CeSR: A Cell State Remapping Strategy to Reduce Raw Bit Error Rate of MLC NAND Flash

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Outline

Background and Motivation

Design of CeSR

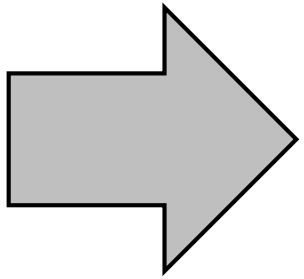
Evaluation

Conclusion

Background and Motivation

NAND Flash:

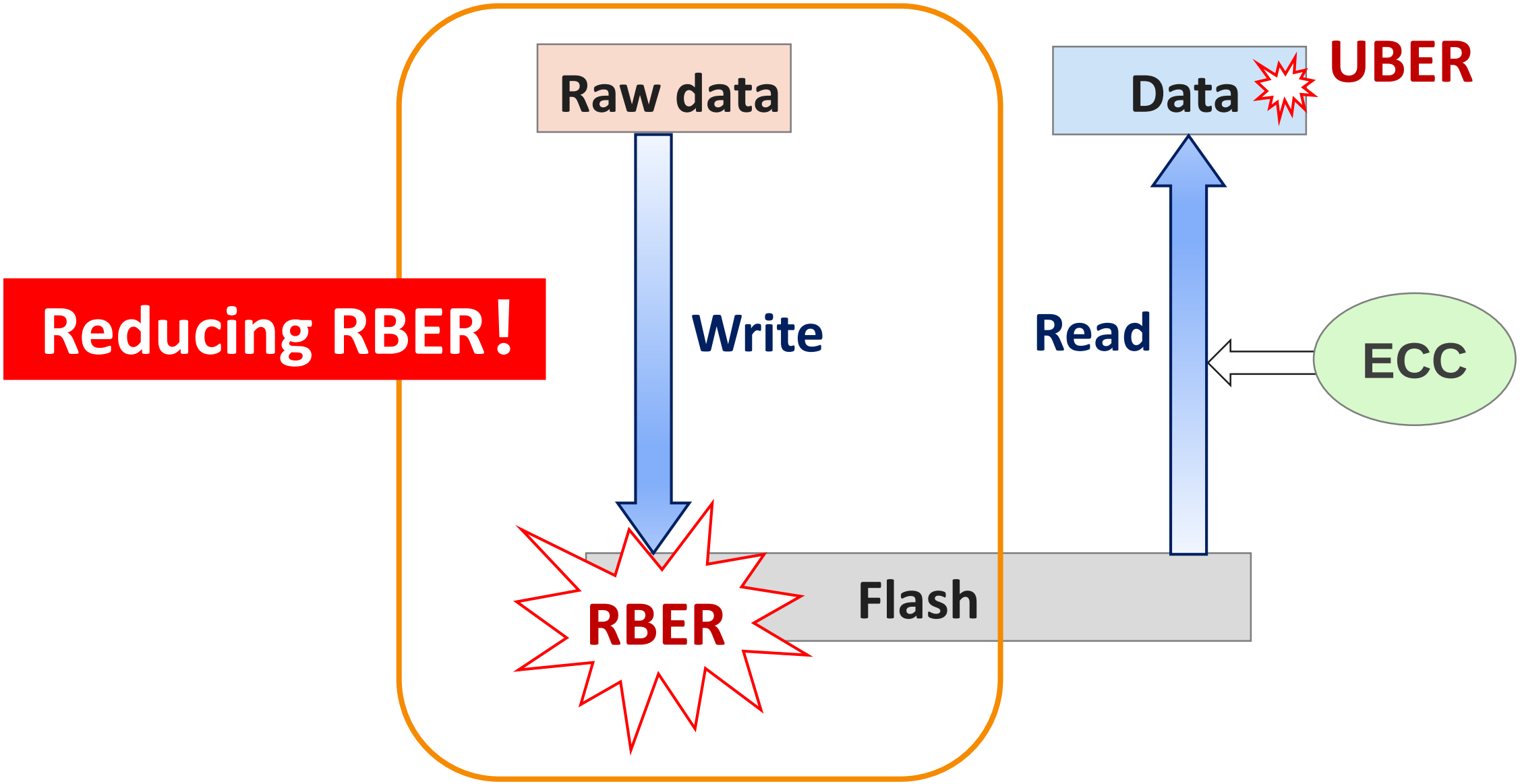
- The size of flash cell decreases
- SLC → MLC → TLC
- 2D → 3D



Flash reliability decreases!

Reduce flash bit error rate

Background and Motivation



Background and Motivation

Three major ways to reduce RBER:

① Read reference voltage optimizing

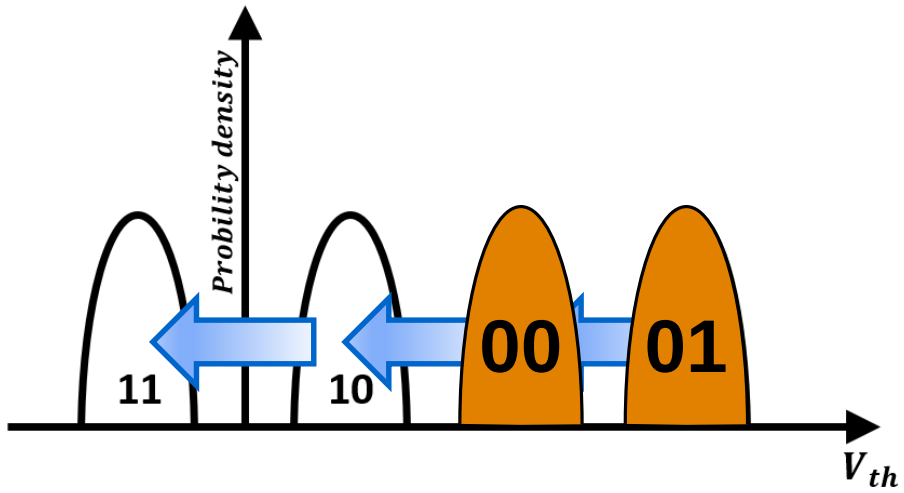
② Flash refreshing

③ Data preprocessing

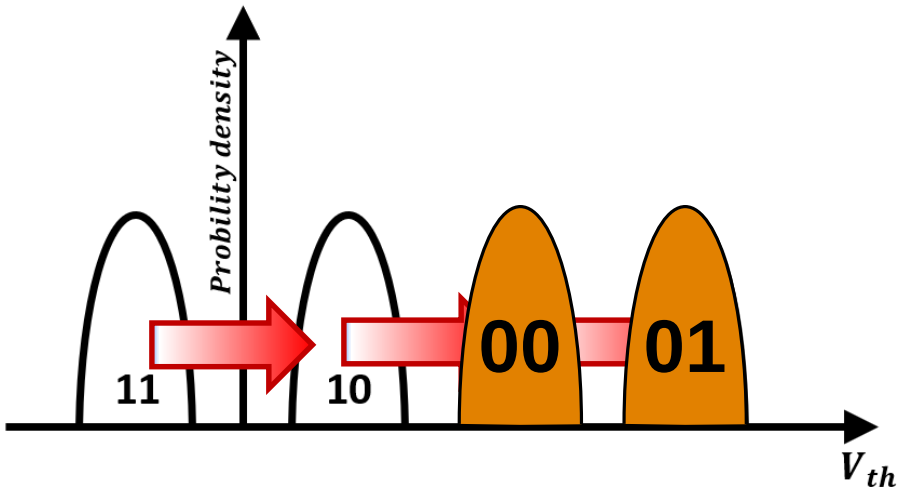
Background and Motivation

Two dominant error types :

Retention error:



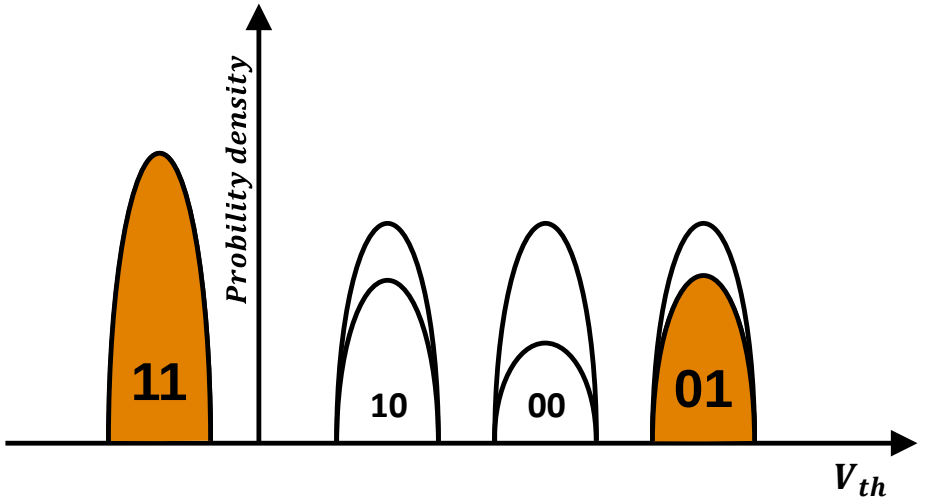
Program interference error:



State with higher V_{th} → More errors

Background and Motivation

Existing works (DPA, AC, NRC)： **increase 1's ratio**

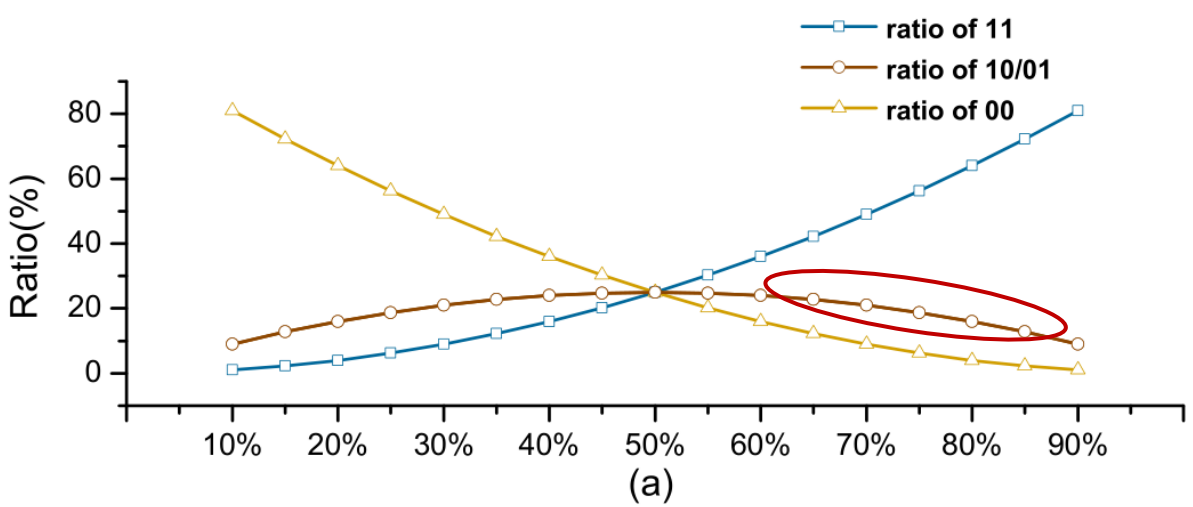


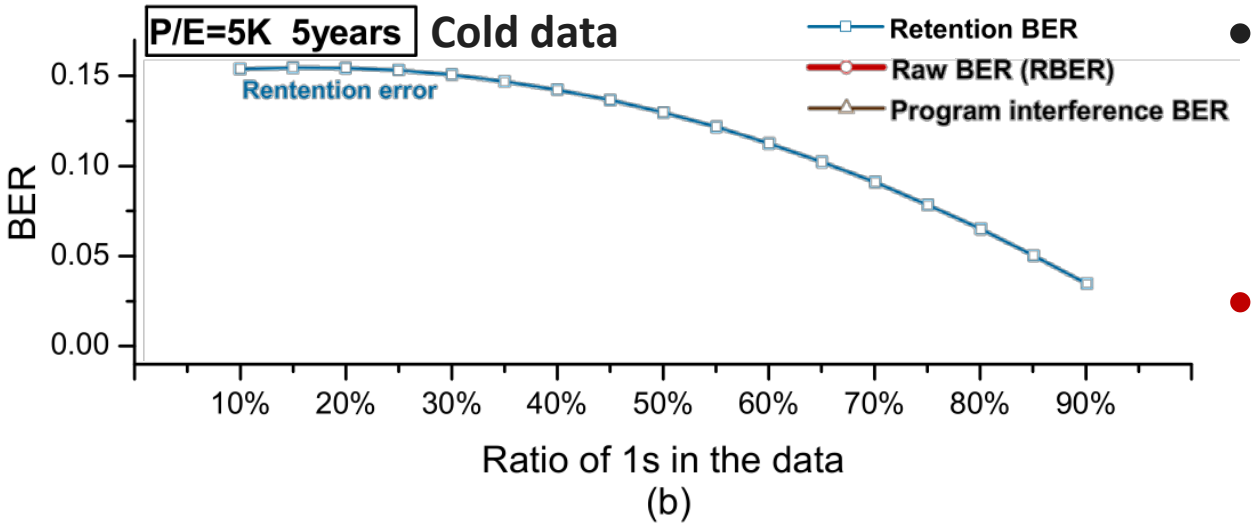
However:

① **Decreasing** the ratio of state **"01"** is also important.

② They consider these two types of errors **separately**.

Background and Motivation





- The ratio of state “01” doesn’t decrease significantly.
- Retention errors of cold data are still serious.
- Increasing 1’s ratio does not always reduce the RBER.
- How to adjust the ratio of each state and minimize the ratio of state “01”?

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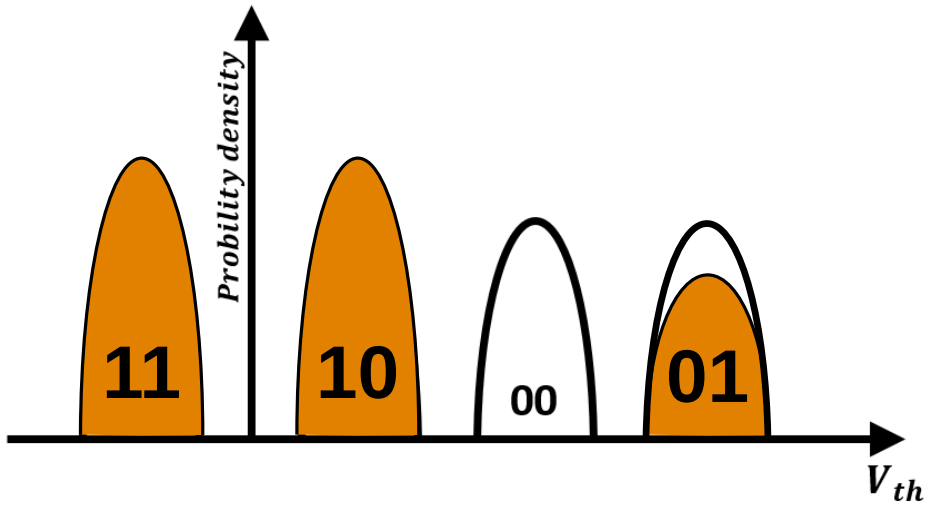
Design of CeSR

The dominant error type of flash is determined by data hotness

- **Hot data**： **program interference errors** are dominant
- **Cold data**： **retention errors** are dominant



Design of CeSR

Data Splitting → Data Flipping → Flag Bits Compressing

Design of CeSR

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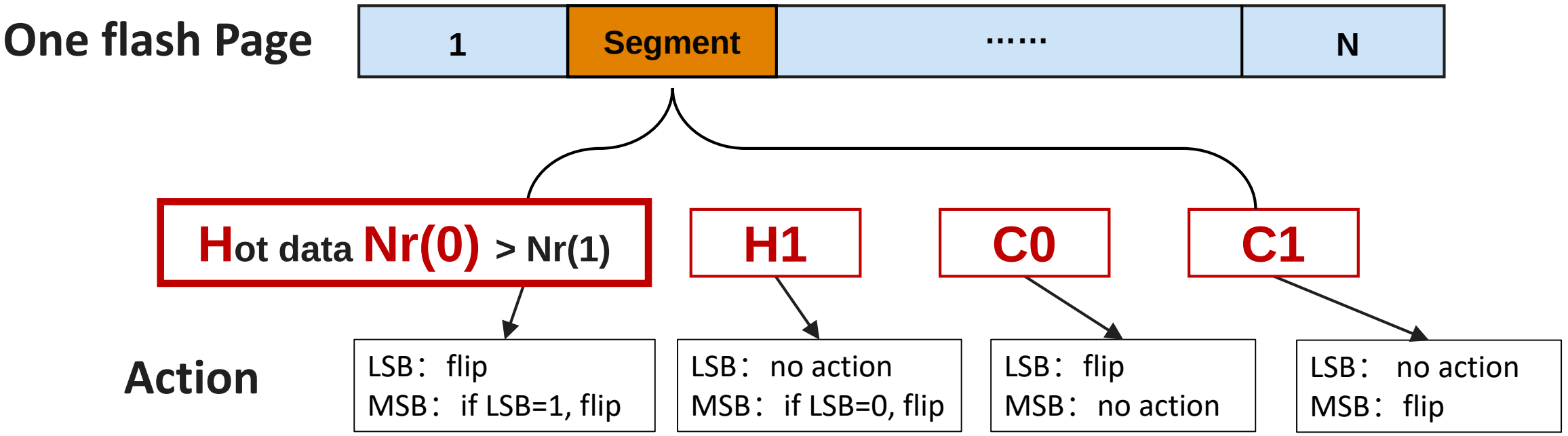
$$Segment\ Size = \frac{Page\ size}{N}$$

Design of CeSR

Data Splitting → **Data Flipping** → Flag Bits Compressing

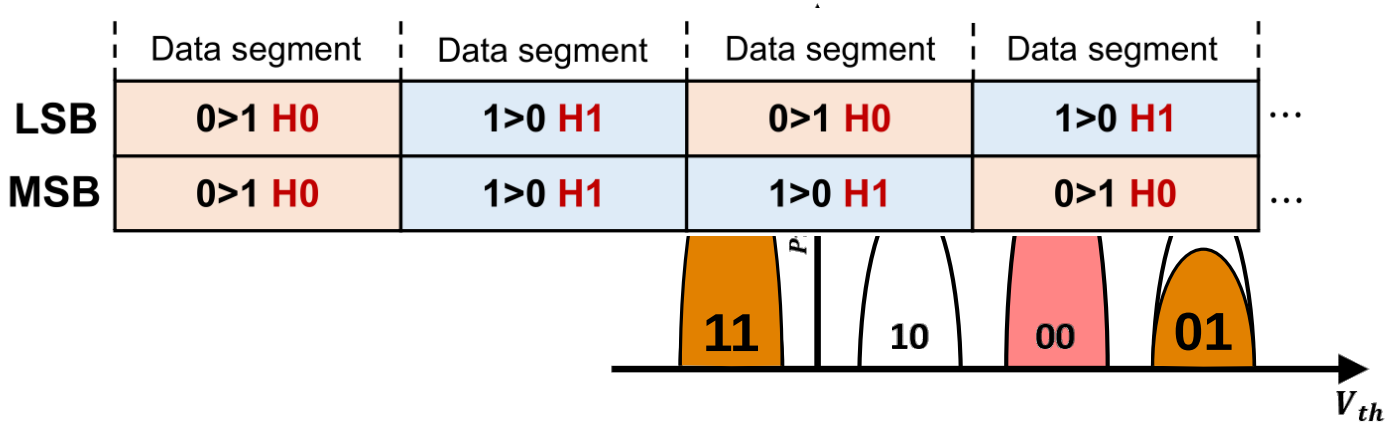
- **Four sub-schemes:**



Design of CeSR

Data Splitting → **Data Flipping** → Flag Bits Compressing

- **Four combinations for hot data:**

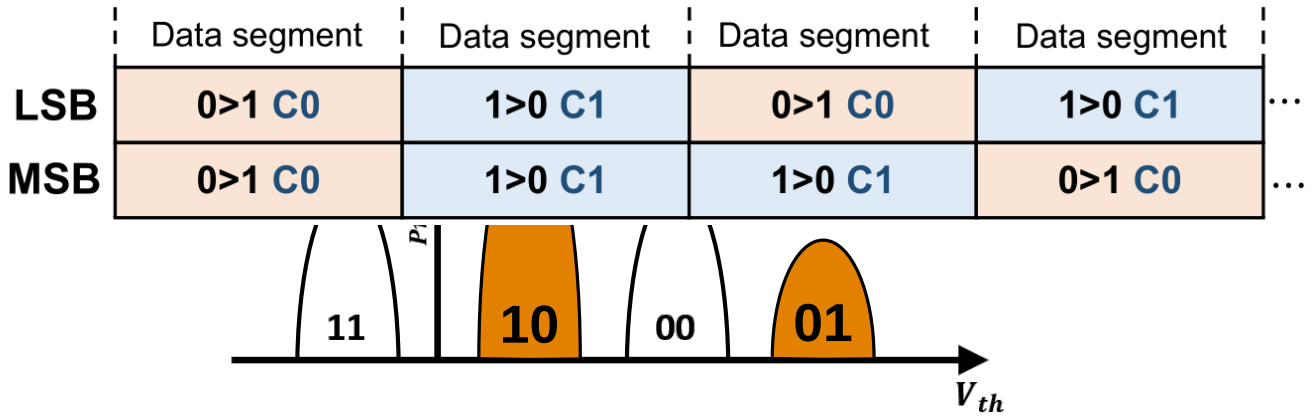


Goal for Hot Data: 11 > 10/00 > 01

Design of CeSR

Data Splitting → **Data Flipping** → Flag Bits Compressing

- **Four combinations for cold data:**

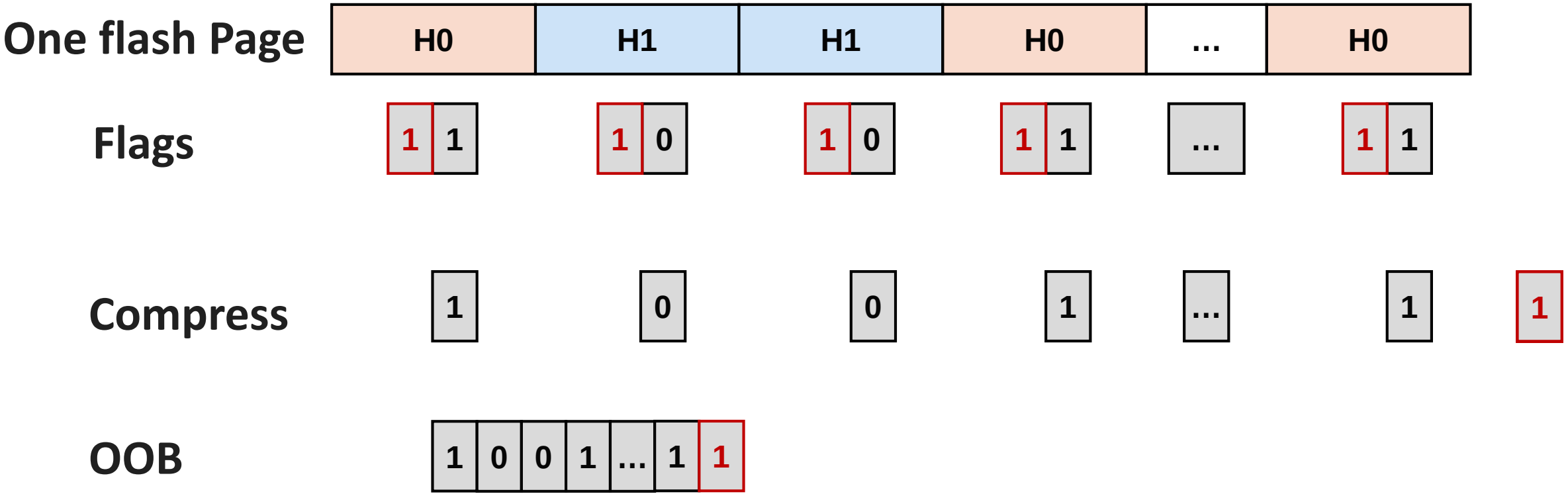


Goal for Cold data: 10 > 11/00 > 01

Design of CeSR

Data Splitting → Data Flipping → **Flag Bits Compressing**

- The **flags** are used to **recover the raw data**.



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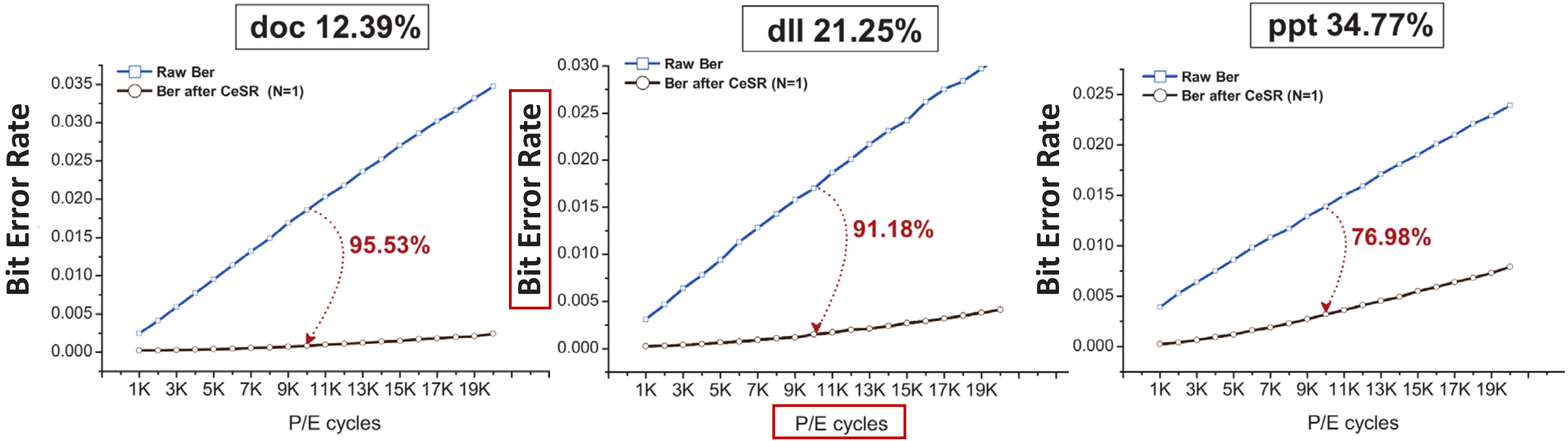
Evaluation

Evaluate the effectiveness of CeSR on hot data

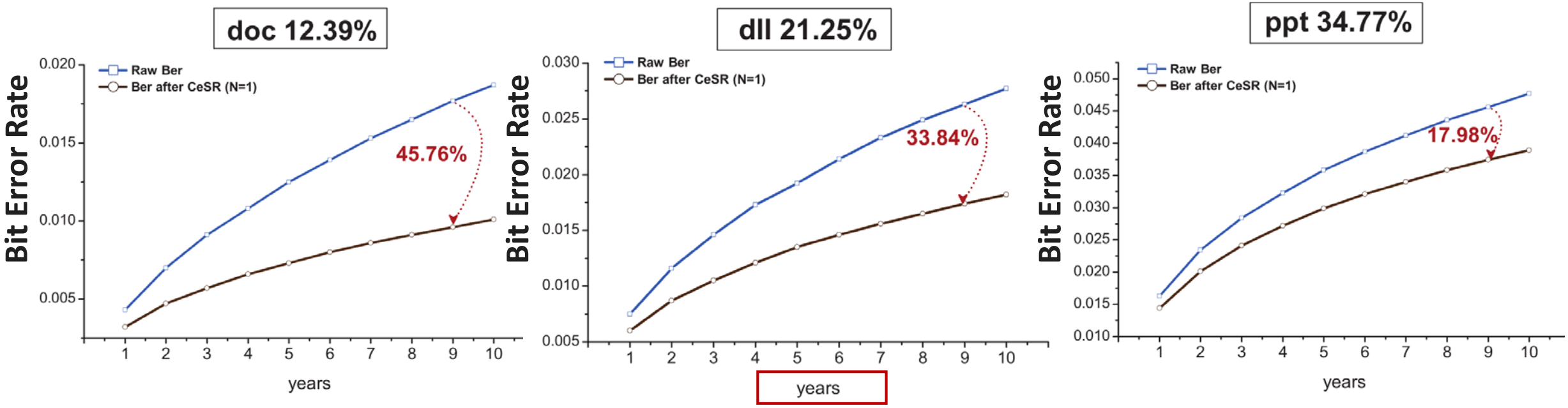
Test under different P/E cycles:



Evaluation

Evaluate the effectiveness of CeSR on cold data

Test under different retention time :

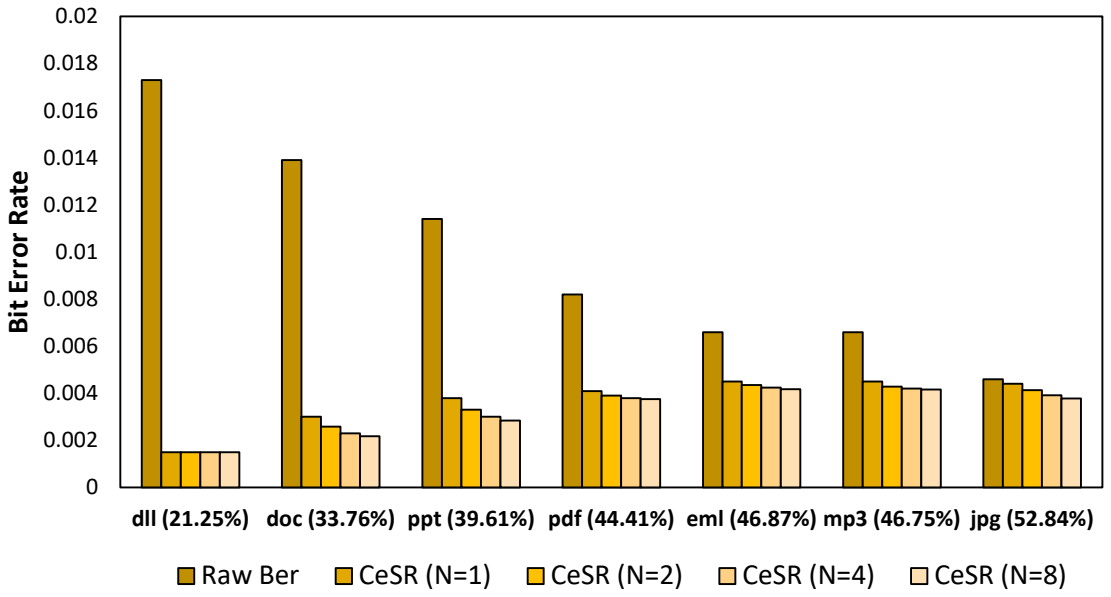


Evaluation

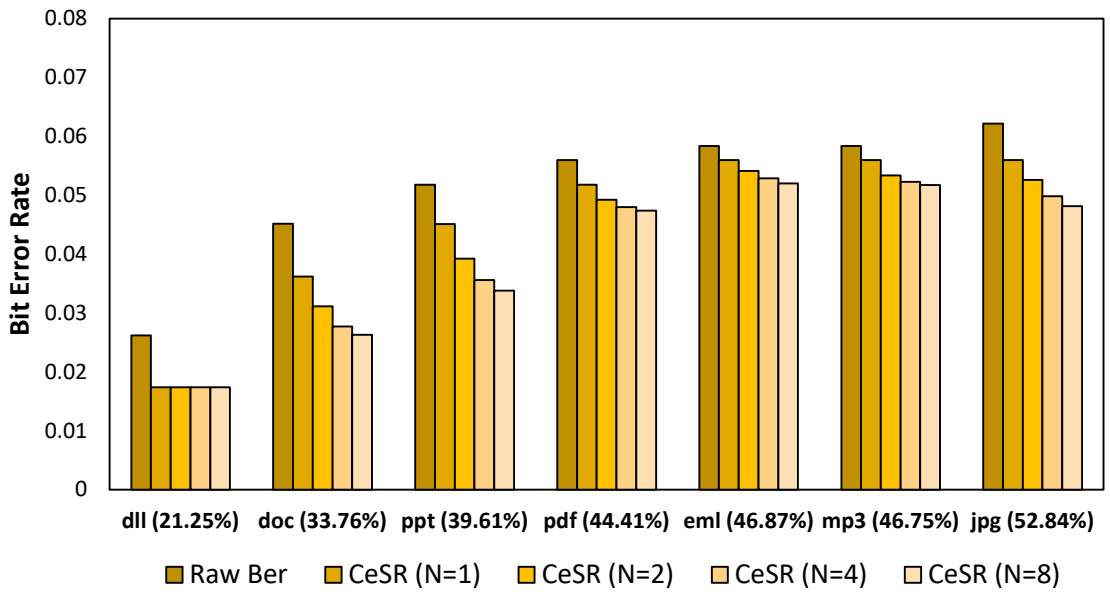
Evaluate the effectiveness of different processing granularities

Test under different data segment length :

Hot data:



Cold data:

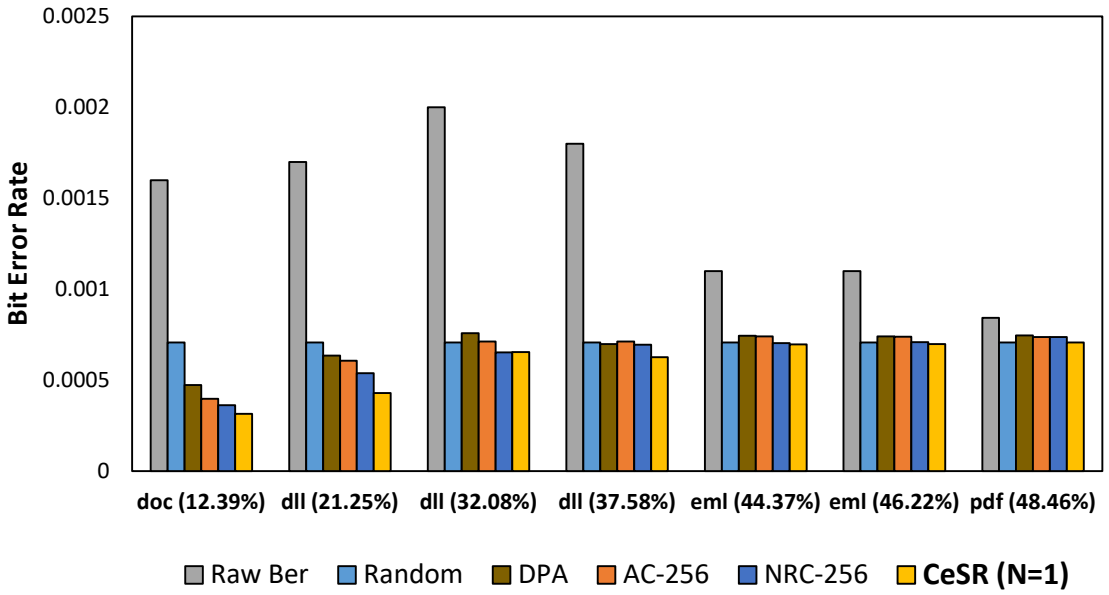


Evaluation

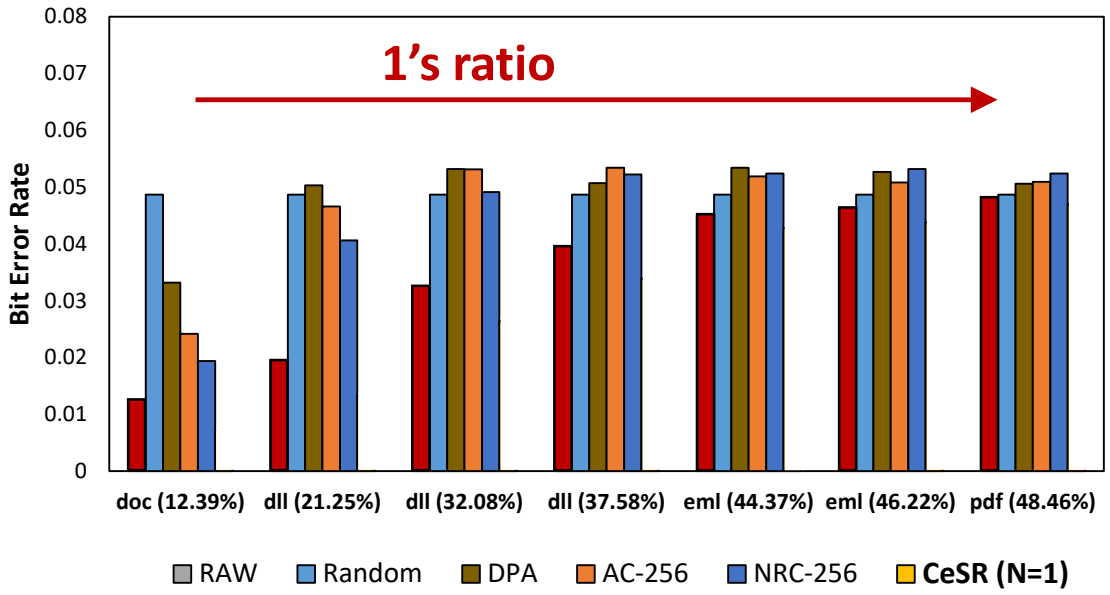
Evaluate the effectiveness of CeSR

Compare with different strategies:

Hot data:



Cold data:



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- CeSR remaps the cell states to adjust the ratio of each state in programming.
- CeSR leverages the counteraction between program interference and retention errors.
- CeSR strategy can reduce the RBERs of hot and cold data by up to **20.30%** and **67.24%**, respectively, compared with the state-of-the-art NRC strategy.

Thank You!

Q & A

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