



Advanced Storage Technology Lab
Xiamen University
(厦门大学先进存储技术实验室)



BitFlip: A Bit-Flipping Scheme for Reducing Read Latency and Improving Reliability of Flash Memory

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36th International Conference on

Massive Storage Systems and Technology (MSST 2020)

Outline

- Background and Motivation
- BitFlip Design
- Evaluation
- conclusion

How errors occur?

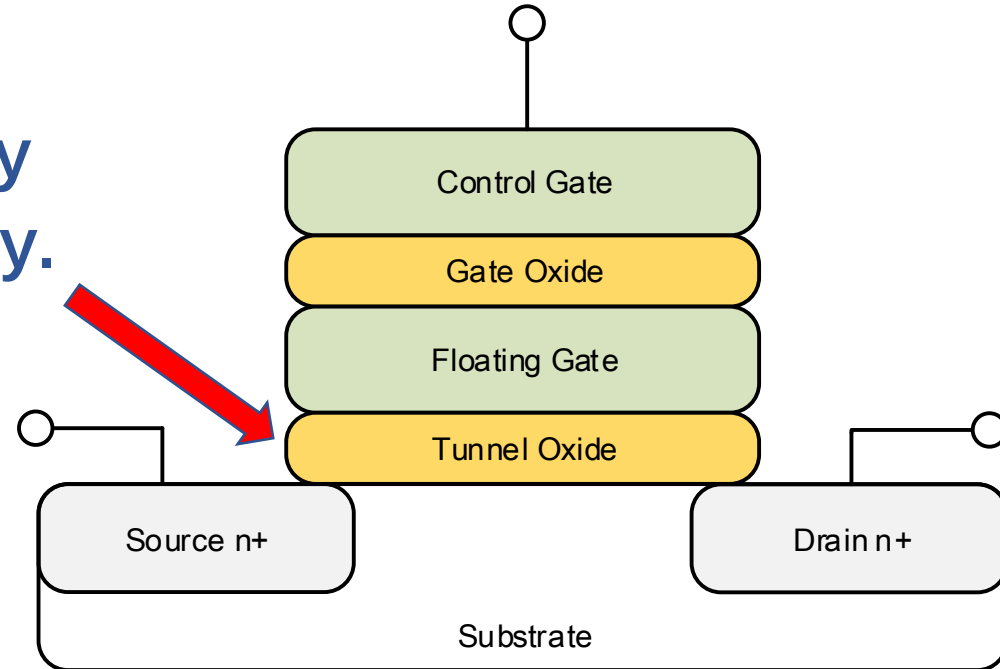
- P/E Cycling Errors
- Program Errors
- Program Interference Errors
- Retention Errors (dominant source of flash memory errors)
-

Our work focus on the Retention errors

Why retention errors occur?

After multiple erase and program operations, the **insulating property of tunnel oxide degrade gradually.**

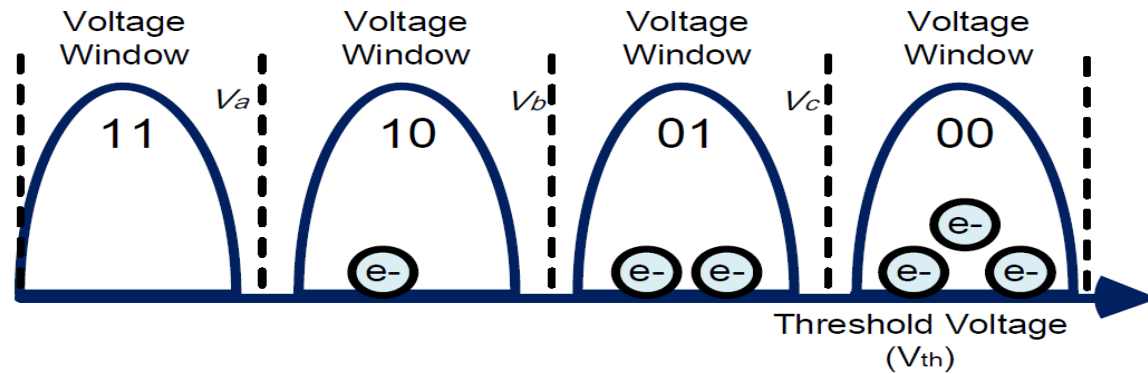
So, more electrons leakage happen and more retention errors occur.



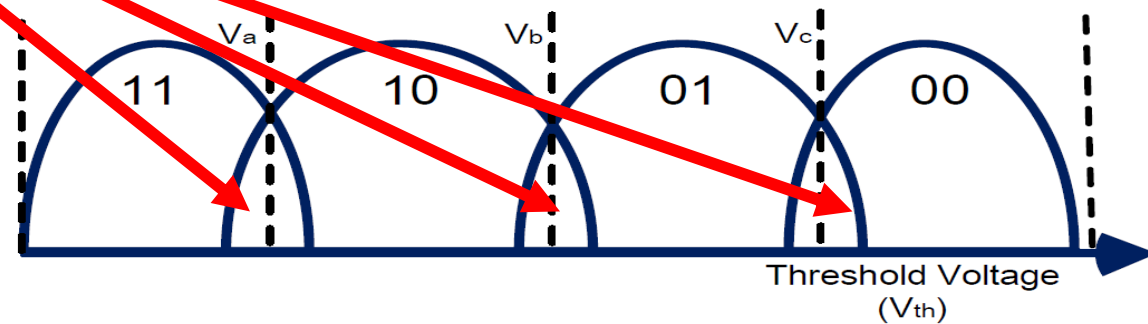
Why retention errors occur?

In MLC cell, there are four states which store four kinds of bits respectively.

Errors happen.

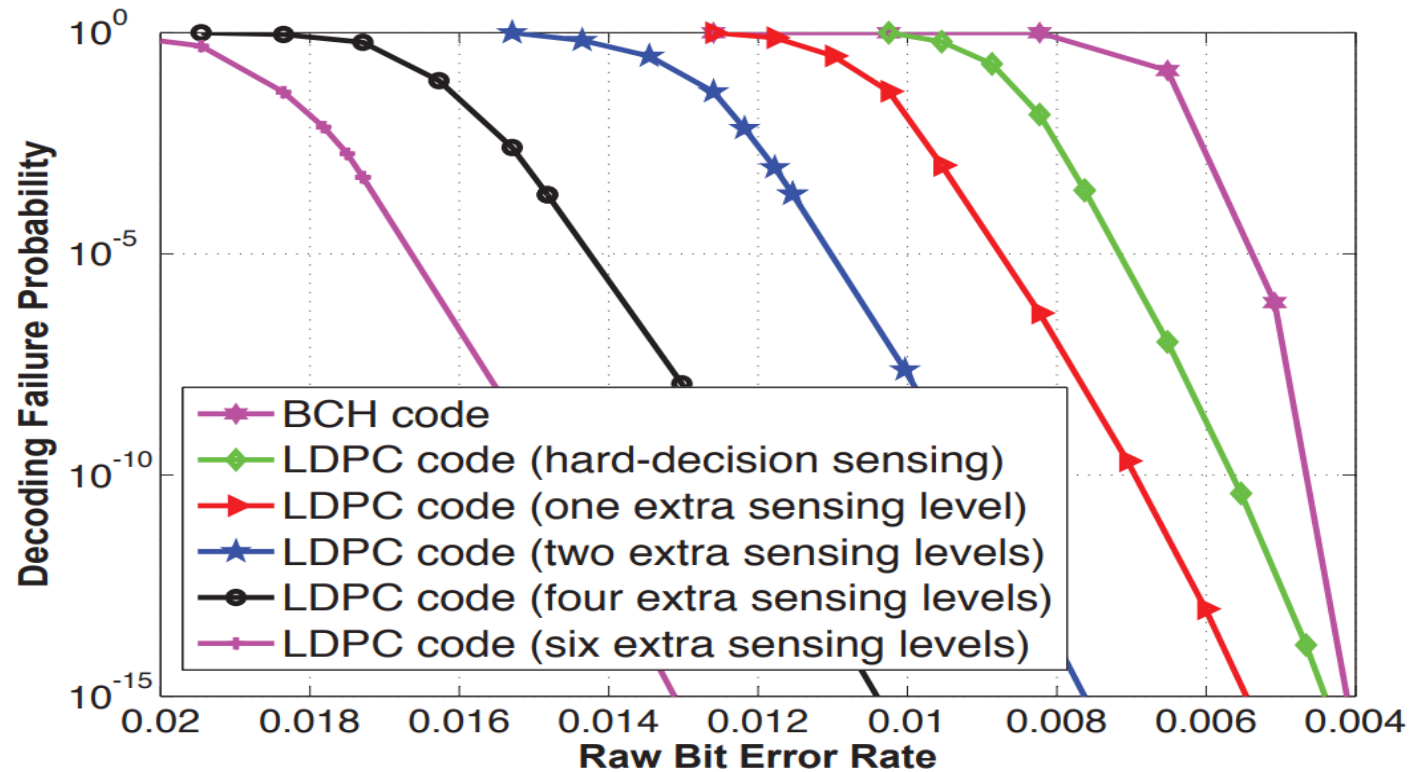


(a) The four voltage windows are non-overlapped.



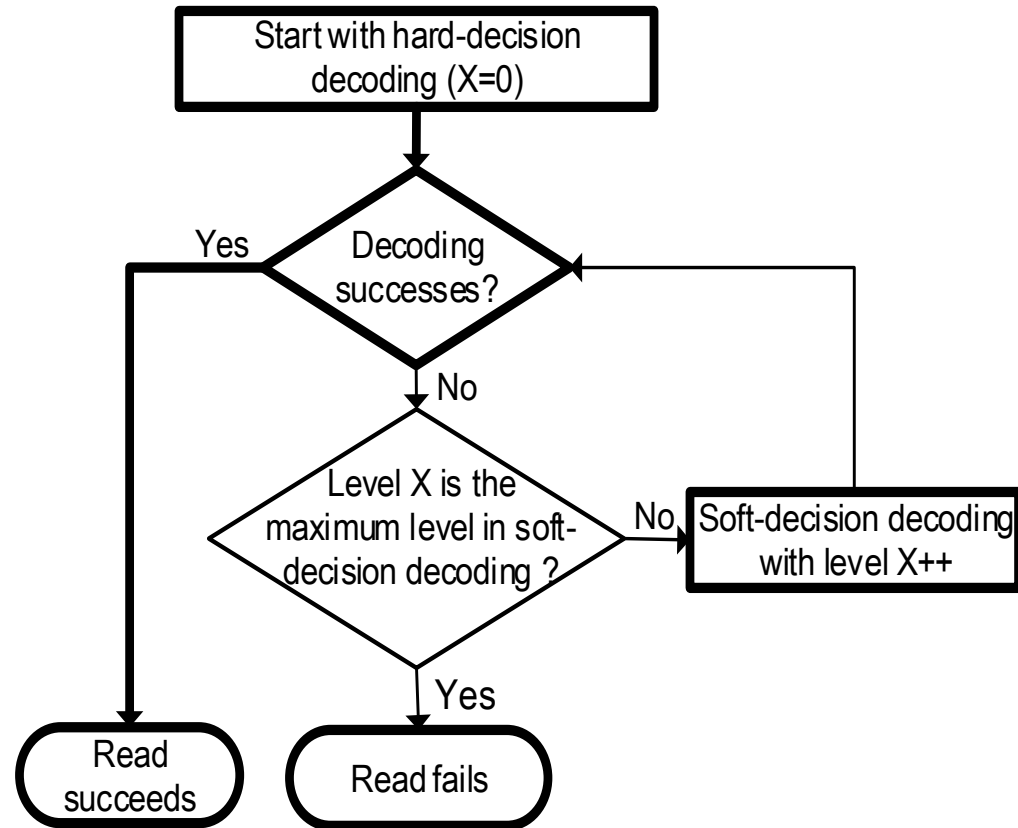
ECC methods in SSDs

LDPC code tolerate more errors, but more errors cause **more sensing level**, which degrade performance.



The figure above from the work of Zhao et al.

LDPC in SSDs



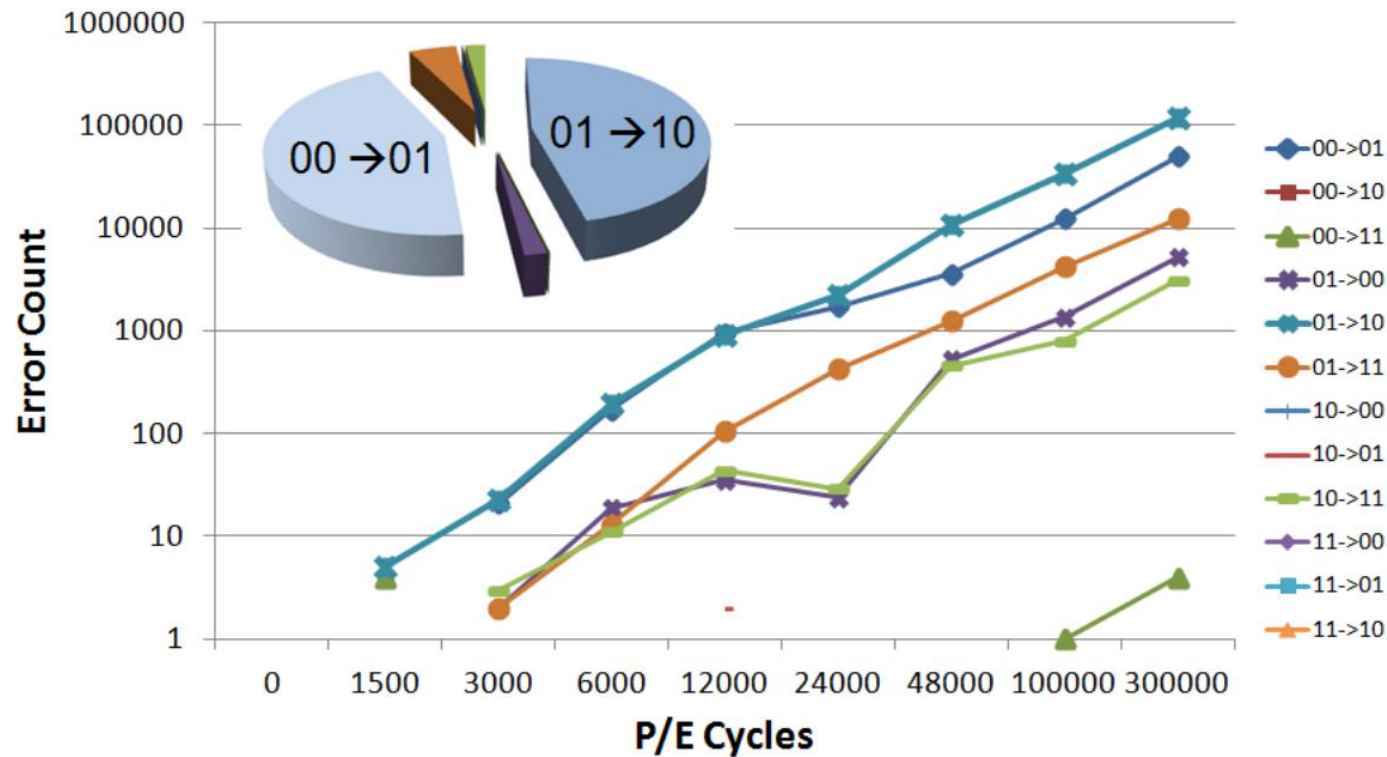
RBERS AND THE CORRESPONDING DECODING LATENCIES.

Level	RBER	Read Latency
Hard-decision decoding	<0.005	$85us$
One extra decoding level	$[0.005,0.006)$	$109us$
Two extra decoding levels	$[0.006,0.008)$	$133us$
Three extra decoding levels	$[0.008,0.009)$	$157us$
Four extra decoding levels	$[0.009,0.01)$	$181us$
Five extra decoding levels	$[0.01,0.012)$	$205us$
Six extra decoding levels	$[0.012,0.013]$	$229us$

Characteristics of retention errors

Most retention errors are 00->01 (46%), 01->10 (44%).

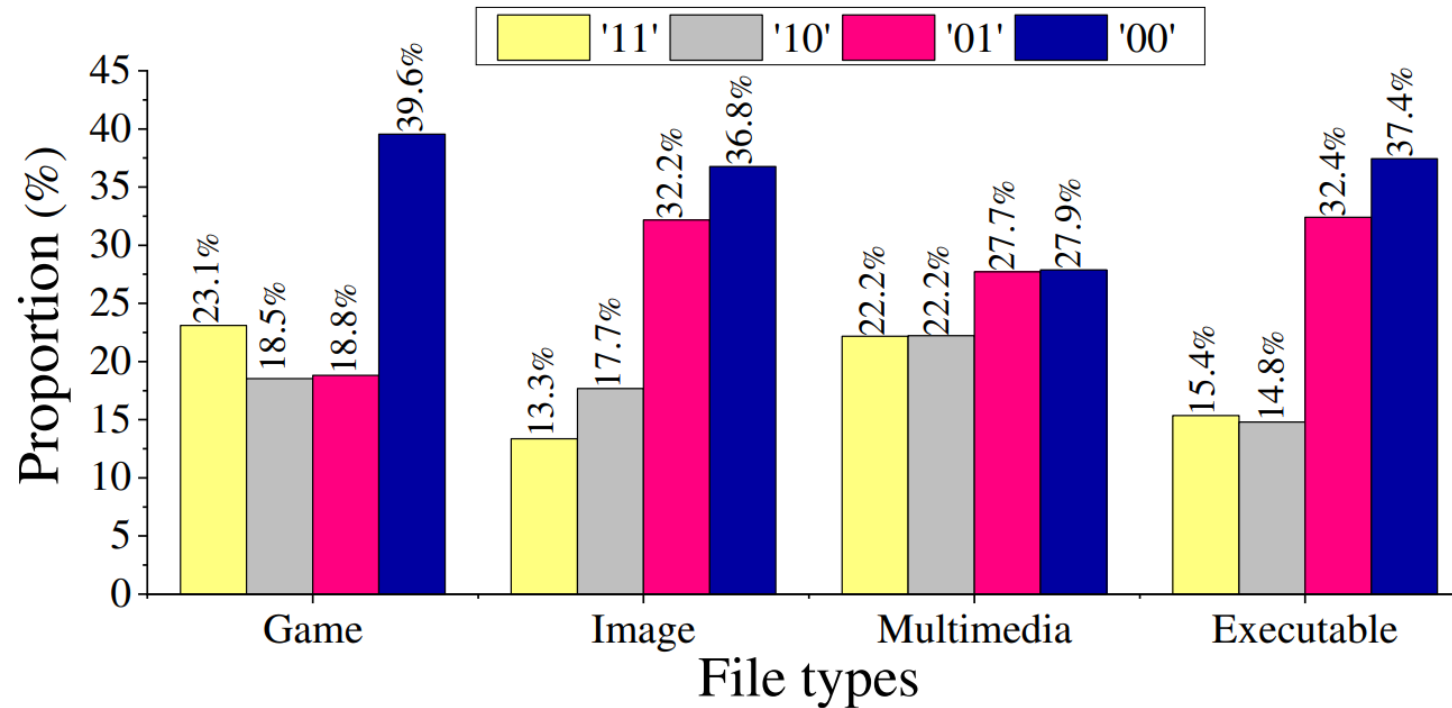
Which means, higher threshold voltages are more likely to leak charge.



The figure above from the work of Cai et al.

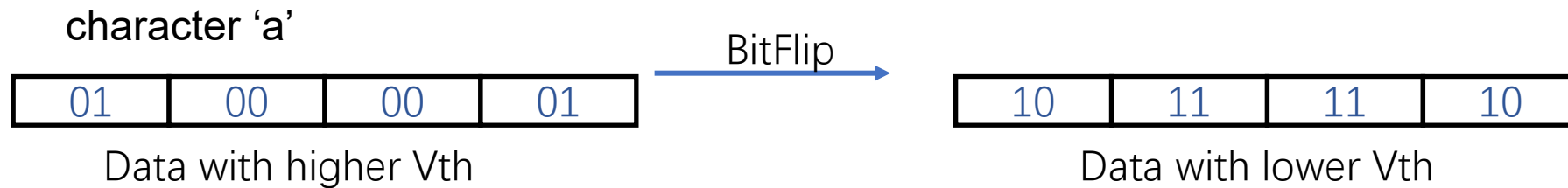
File Analysis

In our analysis, the proportion of four kinds of states are quite different in different files.



Motivation

- So, higher V_{th} (threshold voltages) means higher retention errors.
- Can we reduce the states number with higher V_{th} ?
- We design the **BitFlip**



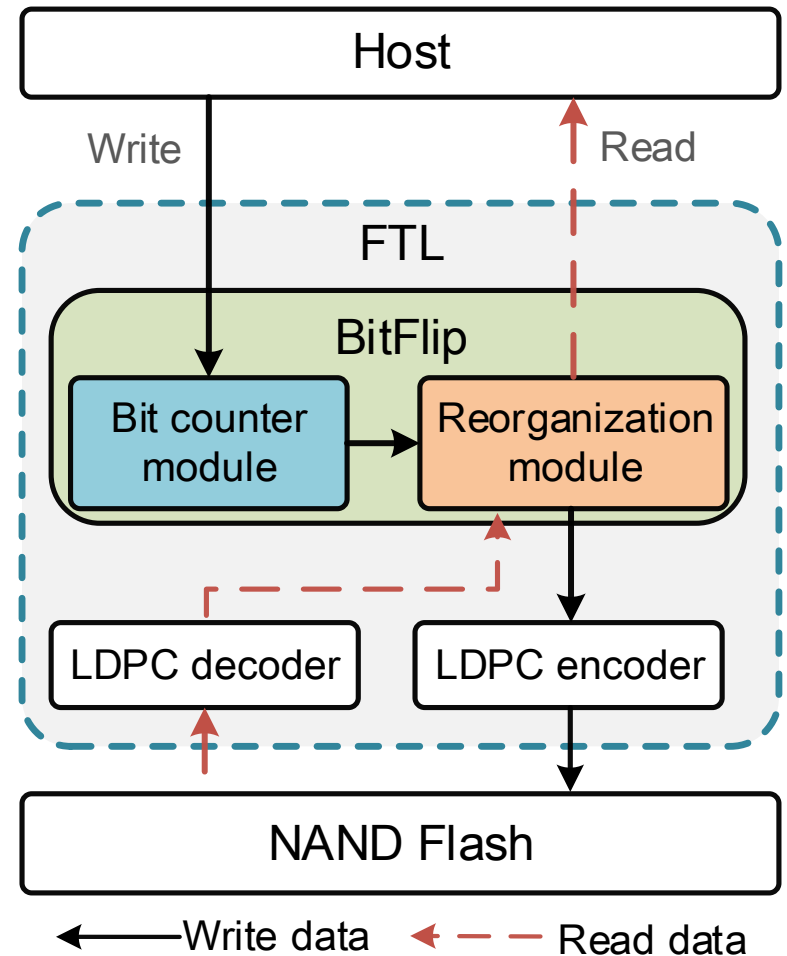
Data store with lower V_{th} states means less errors will occur

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Architecture of BitFlip

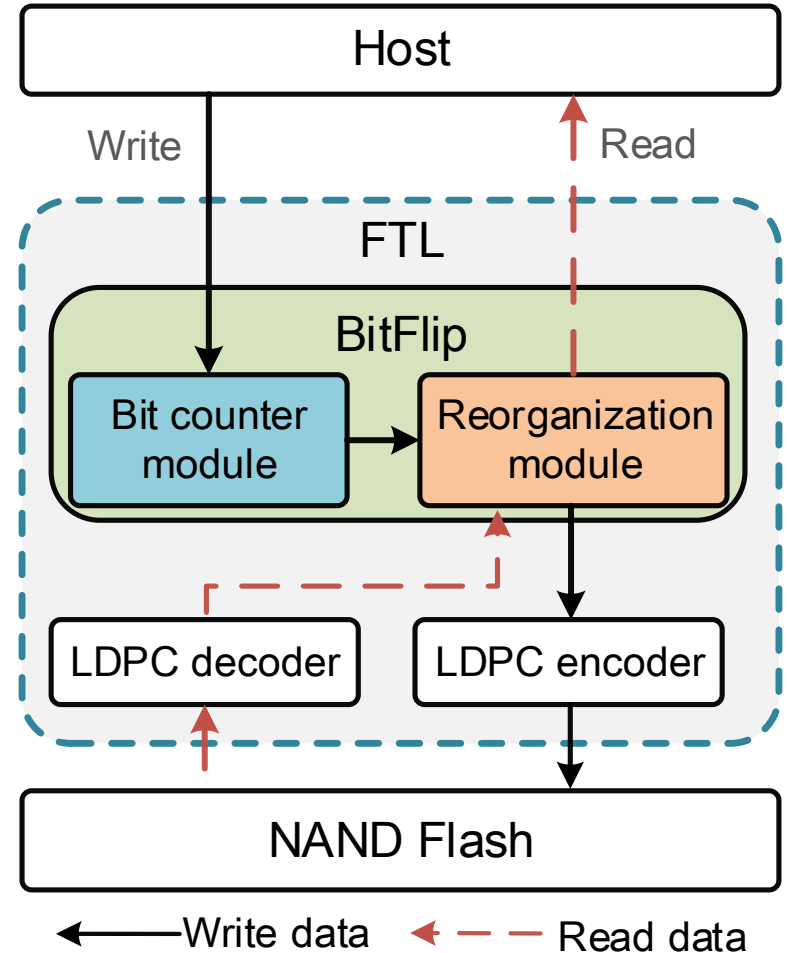
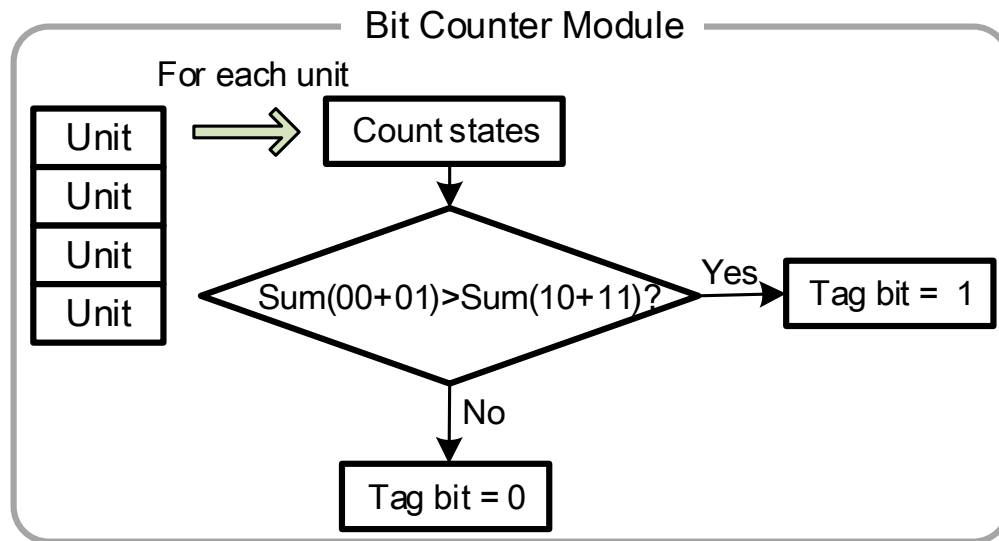
1. BitFlip design in FTL
2. **Bit counter module:** Split a page to equal size units. Calculate the state's number of units to **determine which unit needs to be flipped**
3. **Reorganization module:** Base on tag-bits, flip the units which need flip, then reorganize (data store in Flash)



Write process

1. Bit Counter Module:

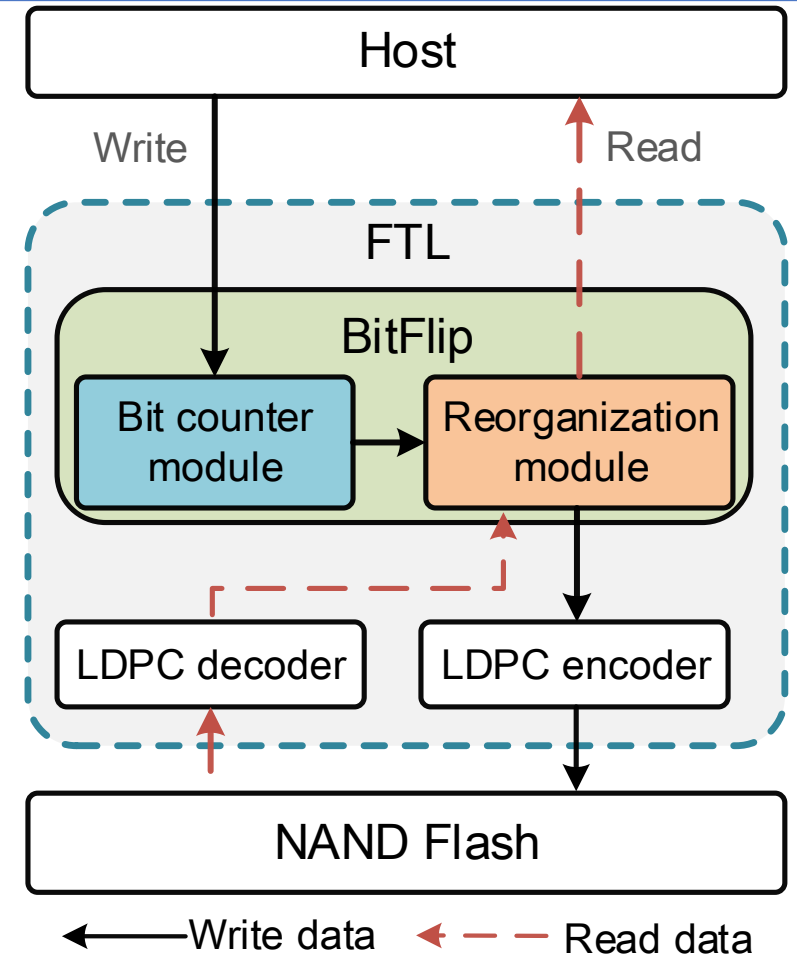
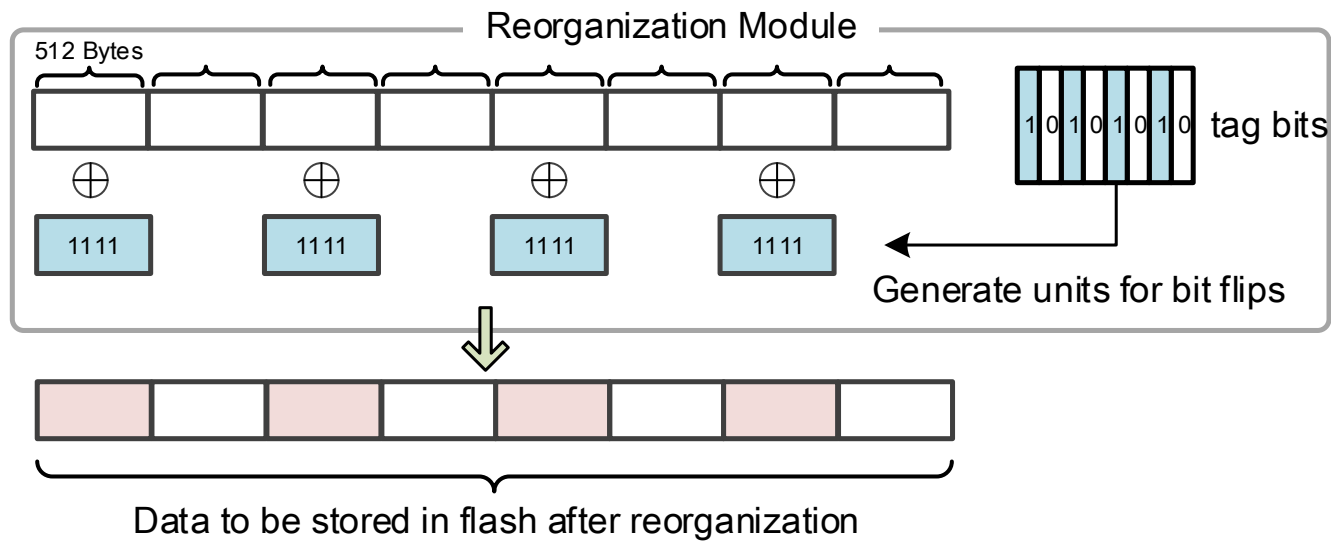
- Split page to several equal units.
- Count states' number of each unit
- Generate tag bit of each unit to mark whether it should be flipped



Write process

2.Reorganization Module:

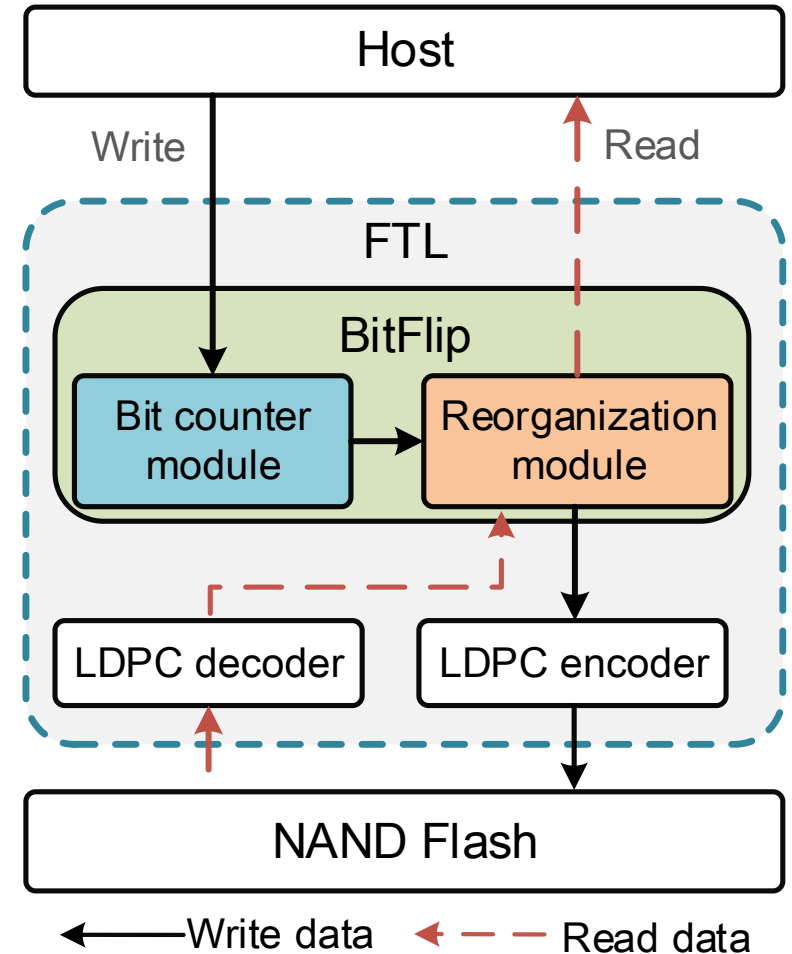
- Judging from tag bits, flip the units and reorganize the units to a page.



Read process

1. Reorganization Module:

- decoding data
- Base on tag bits, flip the units to restore original data



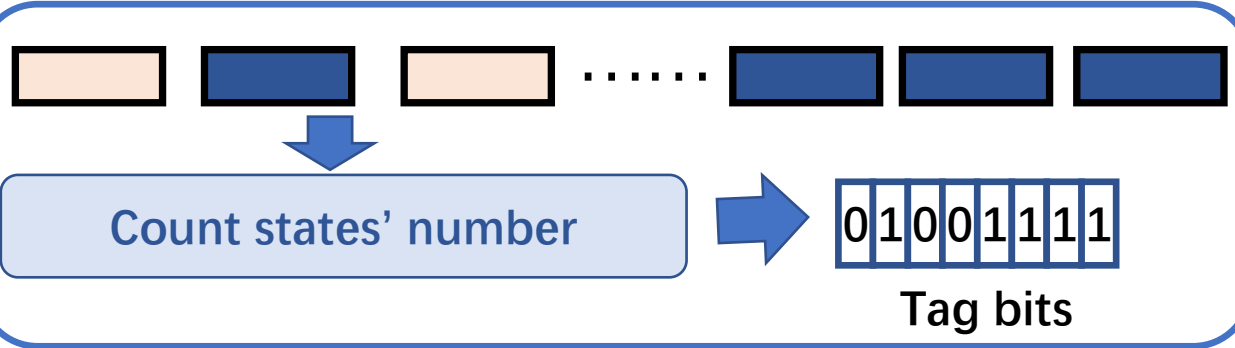
Write

A page



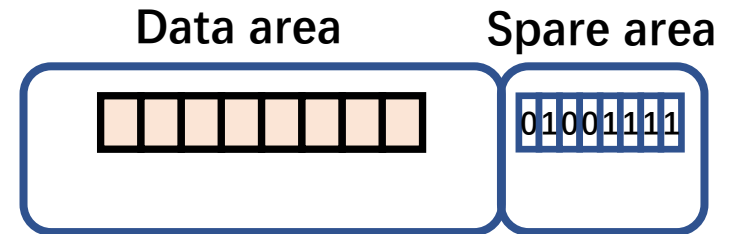
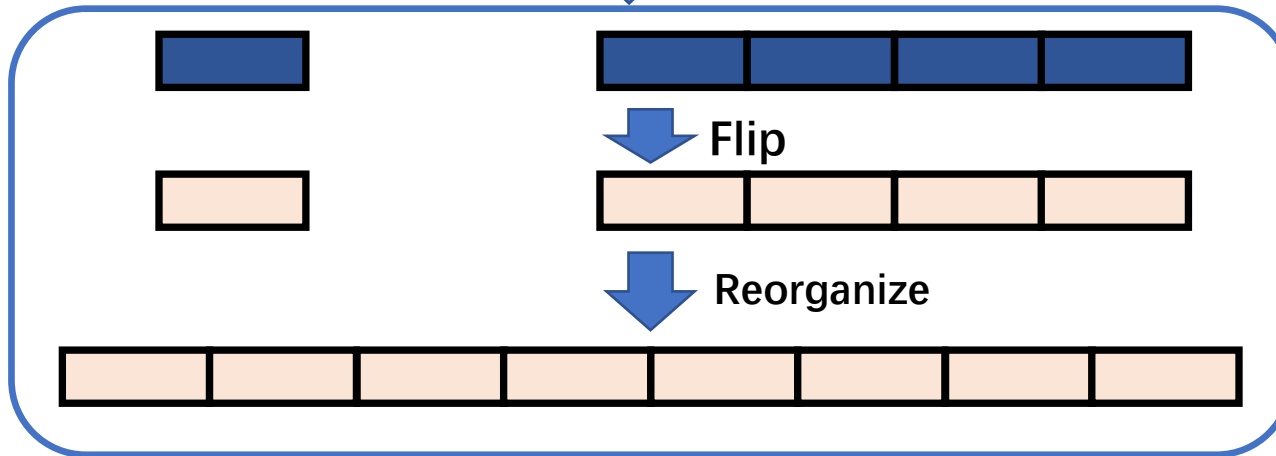
'00'+ '01' > '10'+ '11'

Bit Counter Module

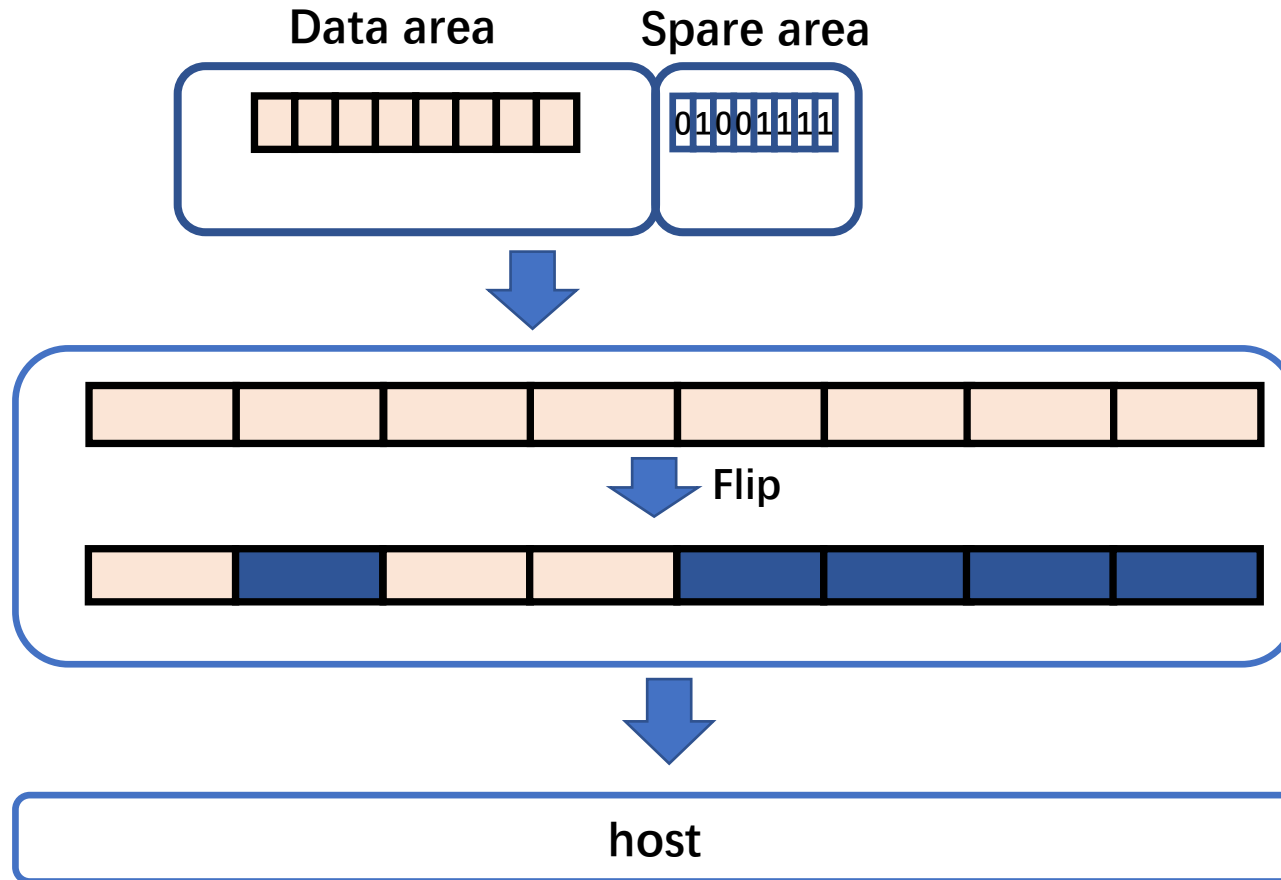


'00'+ '01' < '10'+ '11'

Reorganization Module



Read



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Evaluation Setup

➤ Configurations of SSD

Channels	18	Chips Per Channel	4
Dies Per Chips	2	Planes Per Die	2
Blocks Per Plane	4,096	Pages Per Block	64
Flash Page Size	4KB	Time of Writing a Page	660 μ s

➤ Test environment

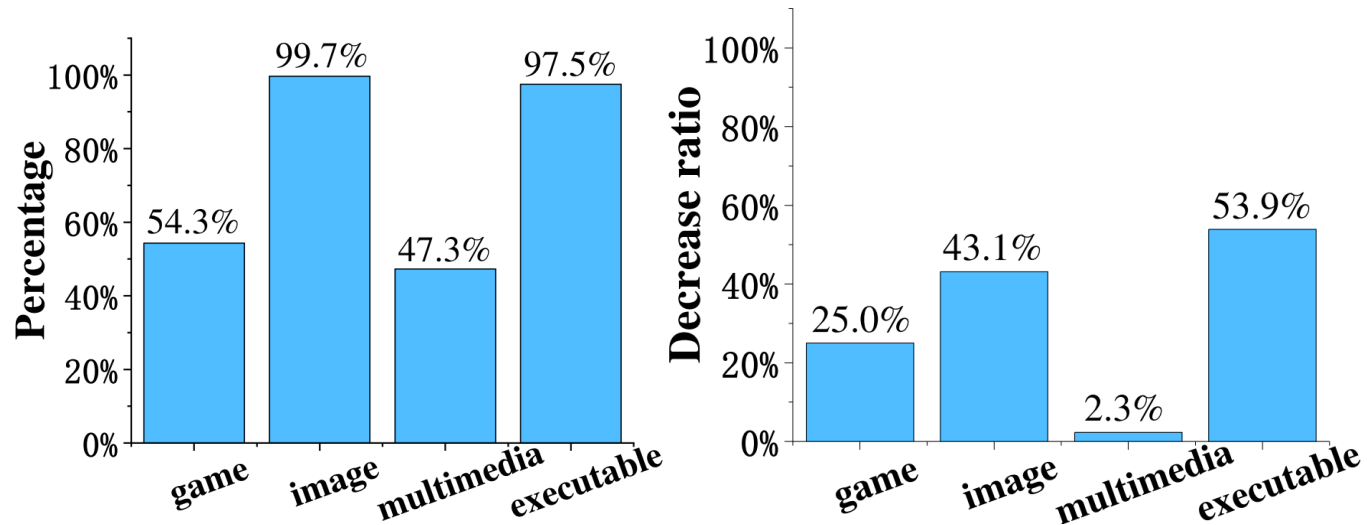
- SSDsim Simulator
- We range the RBER from $4e-3$ to $13e-3$,

➤ Test on real world files and traces files (MSR)

File Type	File information
Game	Kerbal Space Program, Onigiri, Paunch, Robocraft, Sniper Fury, War Thunder, Destiny 2, Dark Deception, Star Conflict, Kaki Raid
Image	Linux (version: 1.1.13, 1.2.12, 1.3.12, 2.0.10, 2.2.21, 2.3.13, 2.4.19, 2.6.12, 3.0.11, 5.0.7)
Multimedia	Photos: KITTI [26] MP4: Vienna New Year Concert (2017~2019) (Bit rate: 128/192 Kbps)
Executable	Executable files (e.g., bash, tar) in the Linux kernel (5.3.0)

Workload	Size of read data (GB)	Read ratio
proj_3	18.23	87.41%
web_1	3.81	85.45%
web_0	17.35	59.78%
hm_0	9.95	32.73%
mds_0	7.37	30.65%
wdev_0	7.15	27.80%
src2_0	1.37	12.76%
rsrch_0	1.39	12%

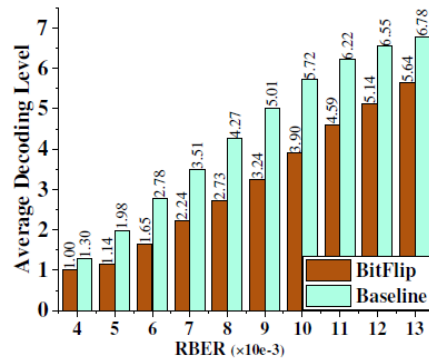
Reduce error-prone states



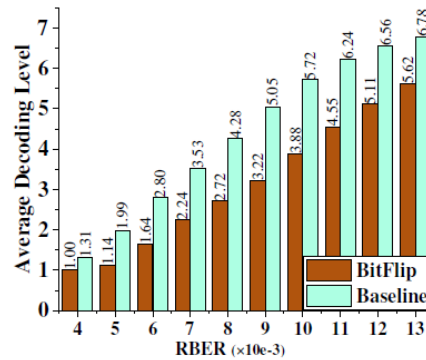
➤ BitFlip can reduce about 2.3%-53.9% of the error-prone states for different file types, thereby demonstrating the effectiveness of BitFlip.

Comparison on the decoding levels

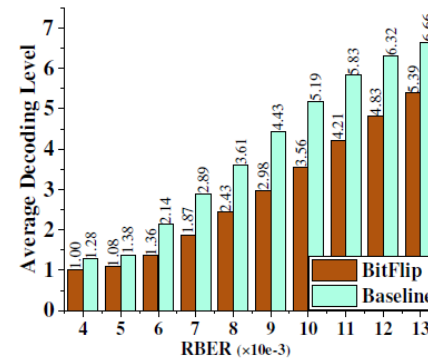
➤ where BitFlip can reduce 27.1%-31.6% of the decoding levels on average.



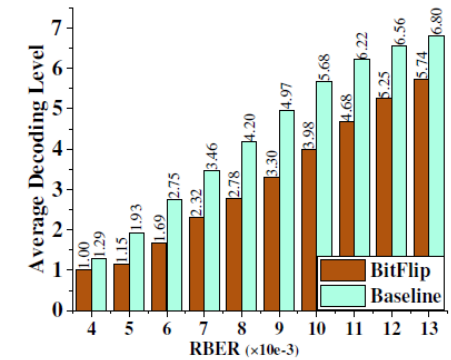
(a) proj_3



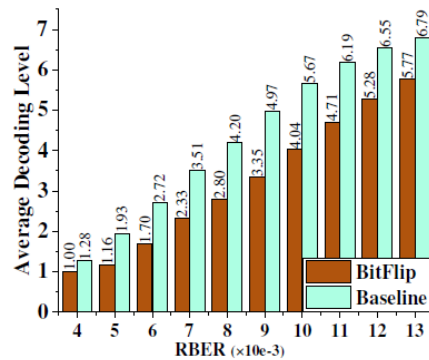
(b) web_0



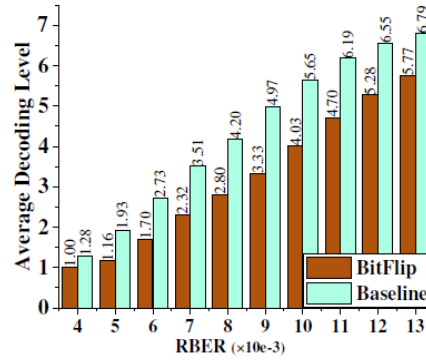
(c) web_1



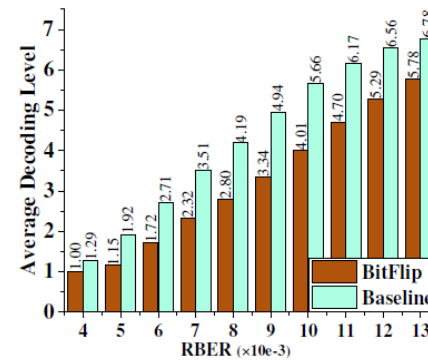
(d) hm_0



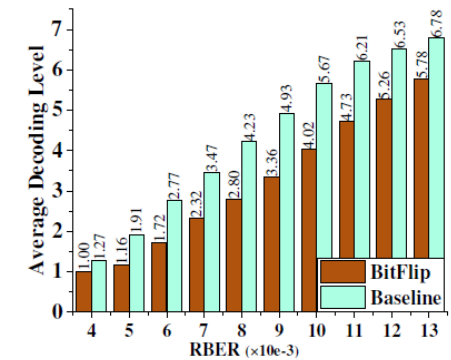
(e) mds_0



(f) wdev_0



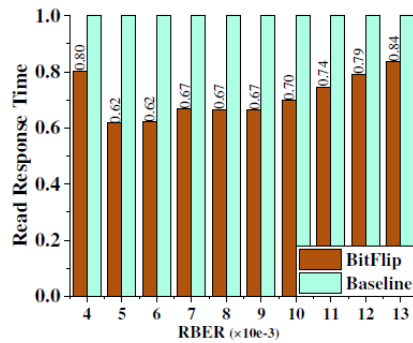
(g) src2_0



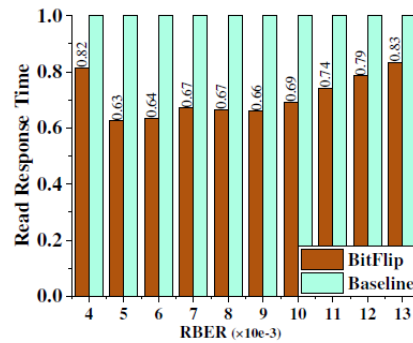
(h) rsrch_0

Comparison on the read latency.

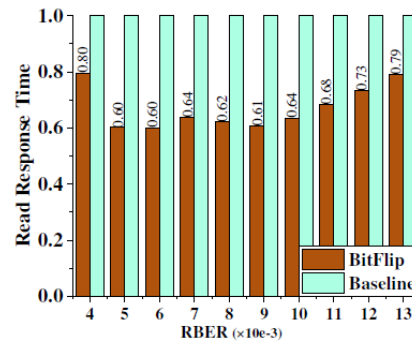
- BitFlip can reduce the read latency by 25.9%-34.2% for each trace compared with the baseline approach.



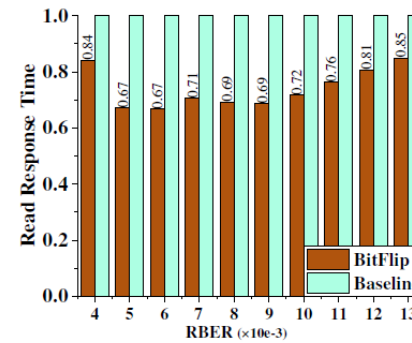
(a) proj_3



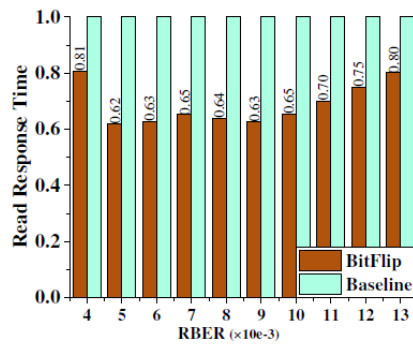
(b) web_1



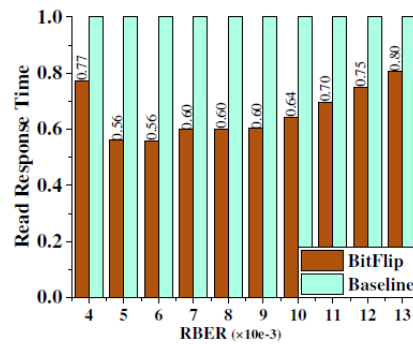
(c) web_0



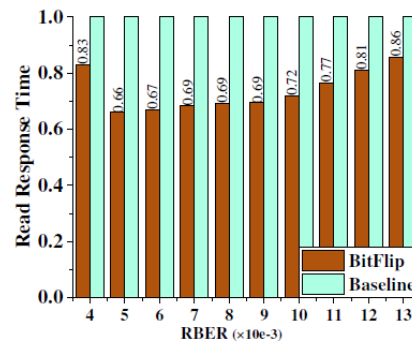
(d) hm_0



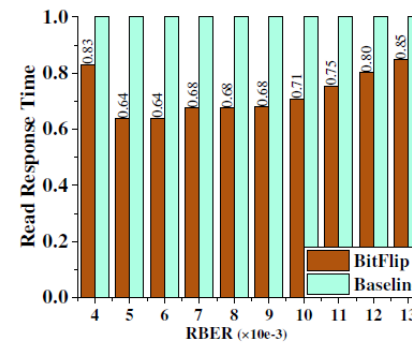
(e) mds_0



(f) wdev_0



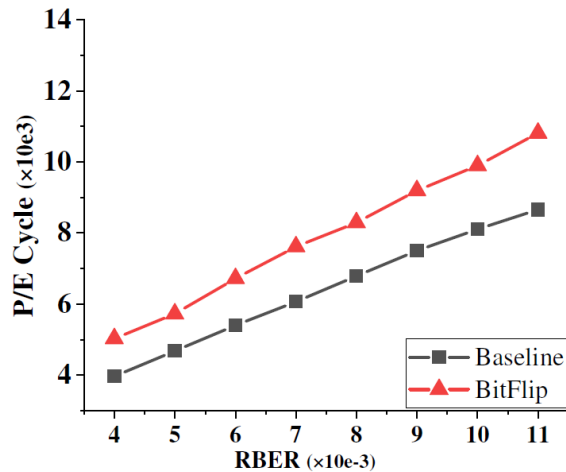
(g) src2_0



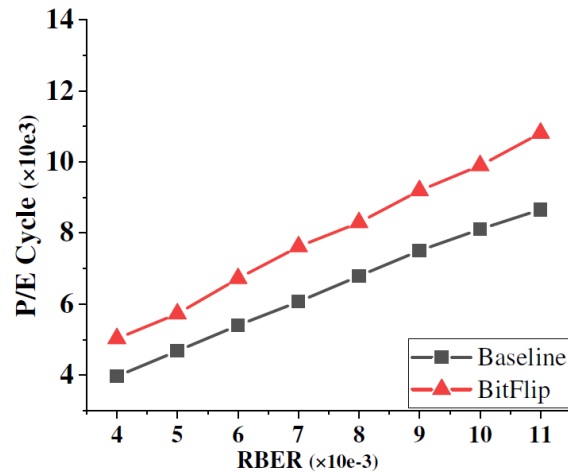
(h) rsrch_0

The number of P/E cycles that can be endured.

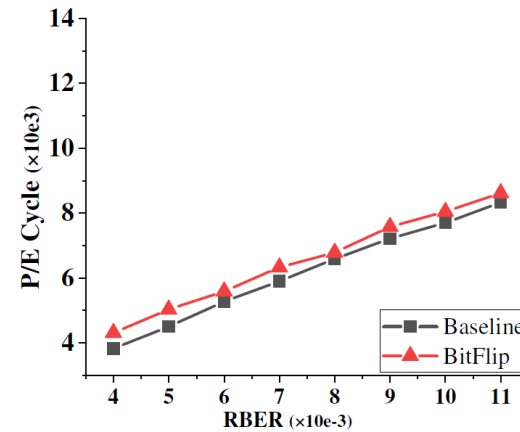
- BitFlip can increase 2.9%-33.3% of P/E cycles that the flash memory can endure.



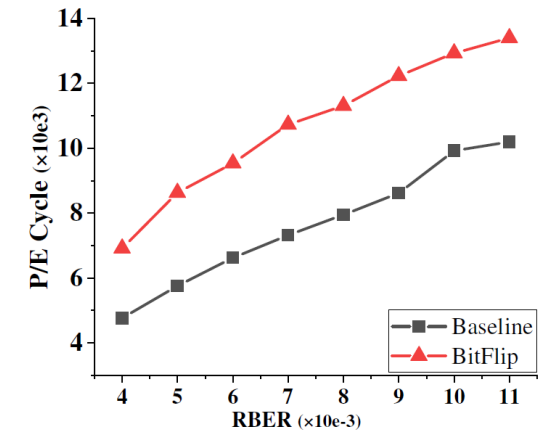
(a) Game files.



(b) Image files.



(c) Multimedia files.



(d) Executable files.

Summary

- BitFlip can reduce the error-prone states
- Comparison on the decoding levels
 - BitFlip can reduce the decoding levels on average.
- Comparison on the read latency.
 - By reducing the error-prone states, BitFlip significantly reduce the decoding time needed in read operations.
- The number of P/E cycles that can be endured.
 - BitFlip increase P/E cycles that the flash memory can endure

Thanks!

Q&A

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